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RFSoC Board Aligns with SOSA Reference Architecture

Pentek's latest RFSoC board puts it on the vanguard of SOSA Technical Standard adoption.

With the launch of its Quartz model 5550 RFSoC board, Pentek stakes out a leadership position in the defense/aerospace sector's adoption of the Sensor Open System Architecture (SOSA) Technical Standard and the reference architecture it defines. To that end, the board implements connector technology that enables a major goal of the SOSA reference architecture—backplane-only I/O. It incorporates the ANSI/VITA 67.3D VPX backplane interconnect standard for both coaxial RF and optical I/O. In addition, the Model 5550 includes a 40-GbE interface and a shelf-management subsystem that are also required by the SOSA reference architecture.

The 3U OpenVPX board, equipped with PCI Express Gen 3 capabilities, comprises an eight-channel analog-to-digital converter (ADC) and digital-to-analog converter (DAC) and is based on the Xilinx Zynq UltraScale+ RFSoC FPGA. It's aimed squarely at applications in communications, electro-optics, electronic warfare, and radar and signals intelligence.

Pentek's modular approach to hardware and software enables quick adaptation to new and changing customer requirements. The Model 5550 uses the Model 6001 QuartzXM eXpress module containing the RFSoC FPGA and all needed support circuitry implemented on a carrier module designed specifically to align with the technical standard for the SOSA reference architecture. This allows for easy upgrades to third-generation RFSoC modules when available.

The Model 5550 is pre-loaded with a suite of Pentek IP modules to provide data capture and processing solutions for many common applications. Modules include direct-memory-access (DMA) engines, DDR4 memory controller, test signal and metadata generators, data packing, and flow control. The board also comes pre-installed with IP for triggered waveform and radar chirp generation, triggered radar-range gate selection, wideband real-time transient capture, flexible multimode data

acquisition, and extended decimation. For many applications, the Model 5550 can be used out-of-the-box with these built-in functions, requiring no FPGA development.

The front end accepts analog IF or RF inputs on eight coax connectors located within a VITA 67.3D backplane connector. After balun coupling to the RFSoC, the analog signals are routed to eight 4-GS/s, 12-bit ADCs. Each converter has built-in digital downconverters with programmable 1x, 2x, 4x, and 8x decimation plus independent tuning. The ADC digital outputs are delivered into the RFSoC programmable logic and processor system for signal processing, data capture, or routing to other resources. A stage of IP-based decimation provides another 16x stage of data reduction, ideal for applications that need to stream data from all eight ADCs.

Eight 4-GS/s, 14-bit DACs deliver balun-coupled analog outputs to a second VITA 67.3D coaxial backplane connector. Four additional 67.3D coaxial backplane connections are provided for clocks and timing signals.

The Model 5550 also uses the VITA-67.3D backplane connector for eight 28-Gb/s duplex optical lanes to the backplane. With two built-in 100 GigE UDP interfaces or a user-installed serial protocol in the RFSoC, the VITA-67.3D backplane interface enables gigabit communications independent of the PCIe interface.

Navigating IP

For cases in which IP development proves necessary, Pentek's Navigator Design Suite streamlines the process. The suite includes the Navigator FDK (FPGA Design Kit) for custom IP and Navigator BSP (Board Support Package) for creating host software applications. The Navigator FDK includes the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. All source code and complete documentation is included. Developers can integrate their IP along with the factory-installed functions or use the Navigator kit to replace the IP with their own. The Navigator FDK Library is AXI-4 compliant, providing a well-defined interface for developing custom IP or integrating IP from other sources.

The Navigator BSP supports Xilinx's PetaLinux on the Arm processors. Users can work efficiently using high-level API functions, or they can gain full access to the underlying libraries including source code. Pentek provides numerous examples to assist in the development of new applications.

Serving as a ready-to-use Quartz development platform, the Model 8257 is a low-cost 3U VPX chassis well-suited for developing applications on Pentek's Model 5550 Quartz RFSoC board. Providing power and cooling to match the 5550 in a small desktop footprint, the chassis allows access to all required interfaces and the Model 5901 rear transition module. The 8257 can be configured with optional real-panel dual MPO optical connectors to support the 5550's dual 100-GbE interfaces and coaxial RF connectors.

Designed for air-cooled, conduction-cooled, and rugged operating environments, the 5550 board starts at $38,745. Options for optical interface, GPS support, and memory are available. Deliveries begin in 3Q 2020. The Navigator BSP and Navigator FDK are priced at $2,500 and $3,500, respectively. Both include free lifetime support.

Pentek Inc., *www.pentek.com*

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