ElectronicDesign.
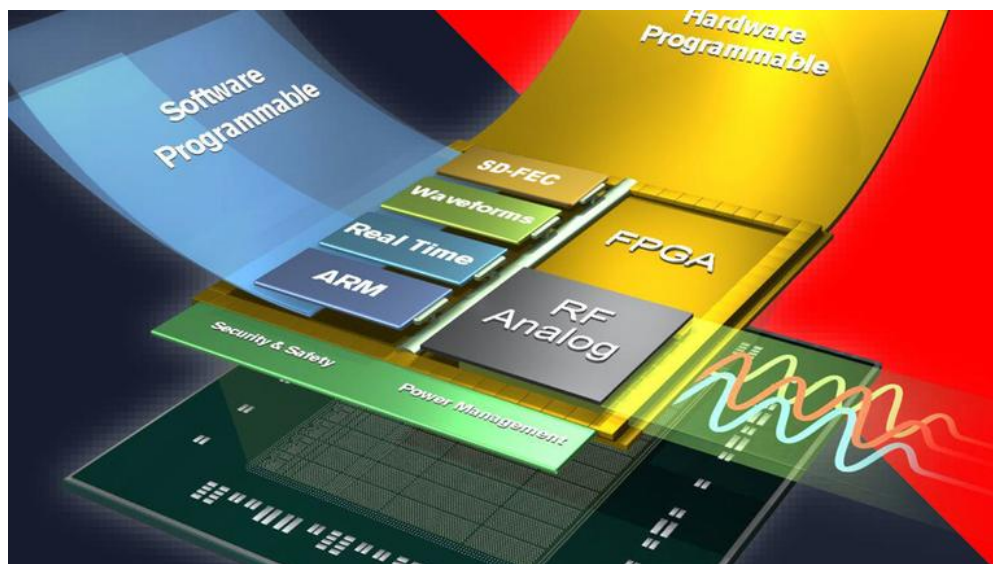
February 20, 2020

By: Bill Wong

RFSoC Delivers FPGA Flexibility with High-Speed RF

Combining high-speed RF with FPGA functionality was never easier or more power-efficient than with Xilinx's RFSoC family.

Xilinx's initial RFSoC release combined the programmability of Zynq Ultrascale+ with RF support that reached up to 4 GHz. The family can eliminate the RF sampling component in many millimeter-wave (mmWave) applications where JESD204 interfaces abound *(Fig. 1)*. Not only does this reduce the parts count, but it cuts out almost 8 W of power for the JESD buffers alone. Bringing the RF inside the FPGA package simplifies system design as well as delivers a higher-performance RF analog connection.
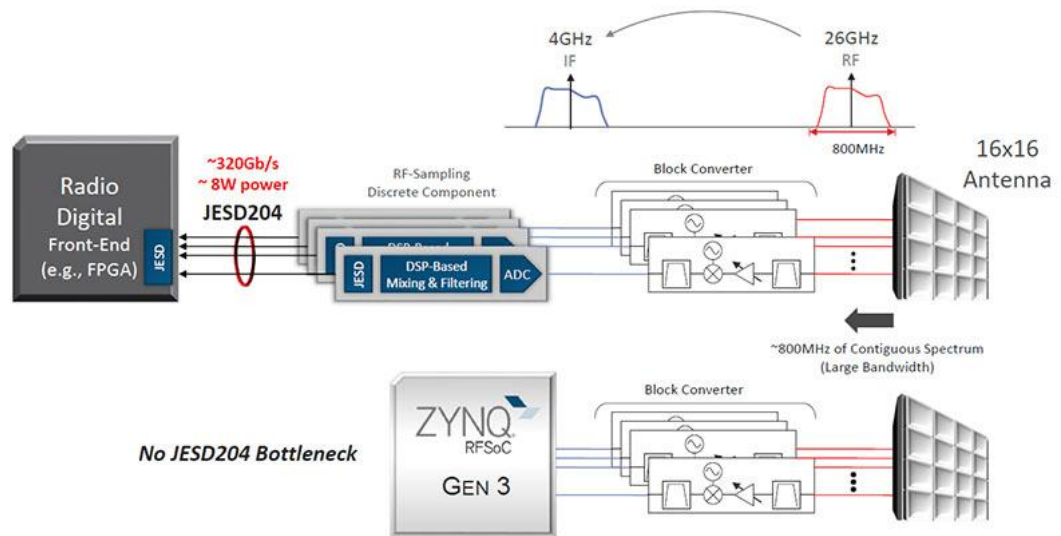
1. Xilinx's UltraScale+ RFSoC incorporates RF sampling into the chip, eliminating the need for buffers to bring in the data plus move the RF components into the chip package.

Another advantage of incorporating the RF inside the chip is that it's possible to analyze the full spectrum and process each band internally rather than having external, fixed signal chains. This provides developers more flexibility for reconfigurable multiband support that would not be possible with fixed signal chains.

The Zynq Ultrascale+ RFSoC Gen 1 has been used in platforms like Pentek's Quartz family. The Model 5950 3U OpenVPX board exposes eight analog-to-digital and digital-to-analog converter (ADC and DAC) channels *(Fig. 2)*. The board also integrates a pair of optical 100G interfaces and a x8 PCIe Gen 3 interface. The RFSoC chip is actually on a Model 6001 QuartzXM eXpress Module with an XMC interface.

2. Pentek's Model 5950 Quartz system is a 3U OpenVPX board with an UltraScale+ RFSoC Gen 1 chip.

The two new announcements in the family are Gen 2 and Gen 3 parts. The Gen 2 parts, available first, bump up the system's RF performance of the system *(Fig. 3)*. They include 16, 12-bit, 2.275-Gsample/s ADCs and 16, 14-bit 6.55-Gsample/s DACs. The UltraScale+ support involves quad-core, 64-bit Arm Cortex-A53 running at speeds up to 1.33 GHz along with a pair of Cortex-R5 real-time processors. The FPGA component has 930K logic elements, 4,272 DSP slices, and 16 33-GHz transceivers. The RF and transceivers are on their own silicon that's linked using silicon

interposer technology. Other off-chip peripheral support includes DDR4-2666 memory and x16 PCI Express (PCIe) Gen 3.
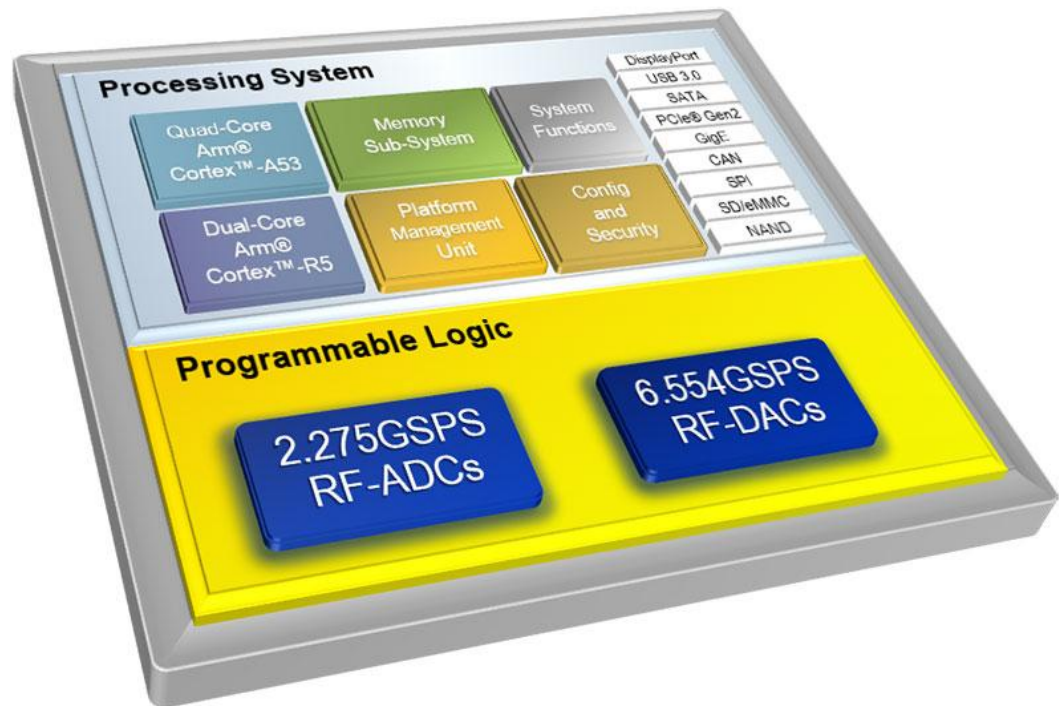
3. The UltraScale+ RFSoC Gen 2 targets 5G with 6.554-Gsample/s RF-DAC and 2.275-Gsample/s RF-ADCs support.

The Gen 3 version *(Fig. 4)* has similar digital and FPGA characteristics but a range of faster ADCs and DACs as well as a hard-core, soft-decision forward-error-correction (SD-FEC) component. The latter is critical to efficient communication protocol handling. On the ADC side, there can be up to 16, 14-bit 2.5-Gsample/s units or up to eight, 14-bit 5-Gsample/s units. On the DAC side, the chips can have up to 16, 14-bit 10-Gsample/s units.
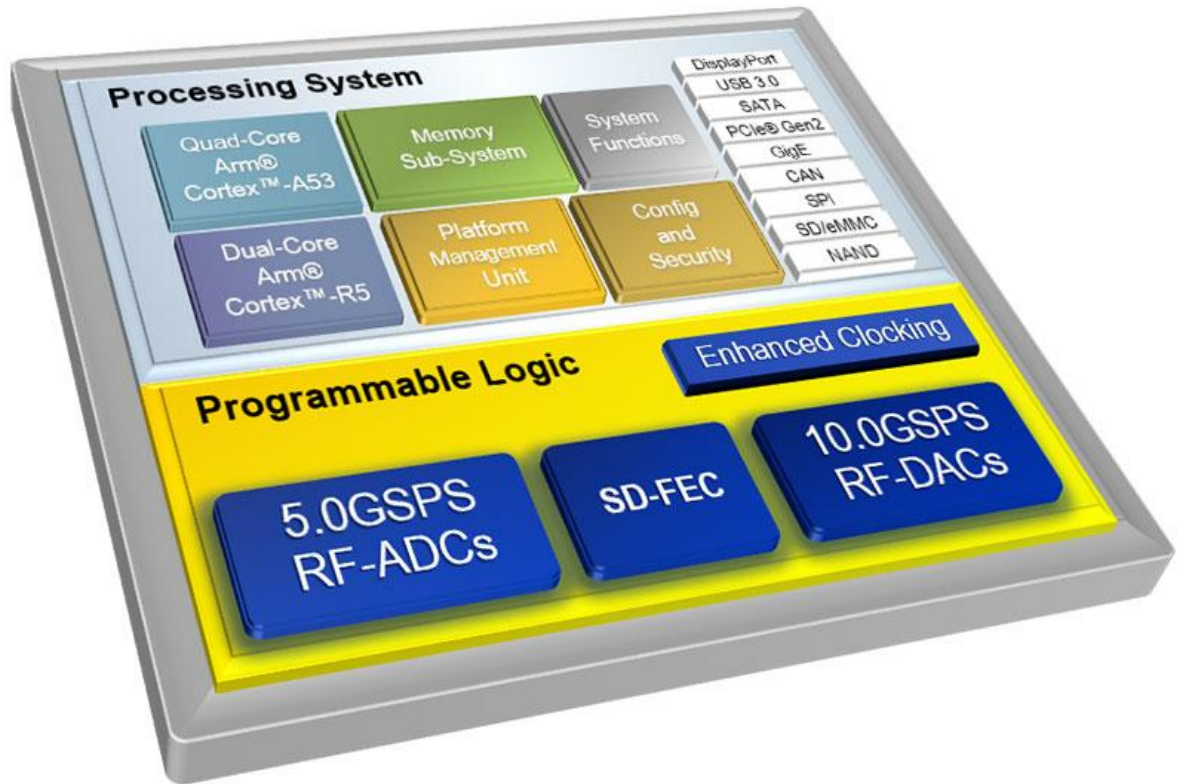
4. With the UltraScale+ RFSoC Gen 3, DAC performance jumps to 10 Gsample/s and it adds a hard SD-FEC block. The chip is also designed to work with external clocks.

The latest UltraScale+ RFSoC parts are just the latest offerings from Xilinx. Its Versal platform, which currently lacks RF support, is on the horizon *(Fig. 5)*.

5.The Versal platform is on the horizon for RFSoC support, which will bring machine-learning acceleration to the table.

The UltraScale+ RFSoC platform provides efficient, high-speed RF support not found in any competing platform. The on-chip computing provides programmatically extensible software support with the flexibility of a high-speed FPGA fabric and high-speed I/O that doesn't have to go through off-chip buffering. The Gen 3 support will offer a larger number of configurations that help it fit into more applications.

https://www.electronicdesign.com/industrial-automation/article/21807610/rfsoc-delivers-fpga-flexibility-with-highspeed-rf