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New Virtex-7 FPGAs boost software radio performance

Software-Defined Radio system performance looks to improve, thanks to the advanced power reduction, increased DSP engines, improved buffering, and faster interfaces of Xilinx's Virtex-7.

By Rodger Hosking
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Wireless appliances in homes, offices, and vehicles … fixed neighborhood broadband wireless networks … the promise of seamless connectivity to the Internet in portable devices, regardless of location: These all drive the explosive demand for improved levels of service in this highly competitive Software-Defined Radio (SDR) market. This crowded radio spectrum means that to be competitive, carriers must squeeze as much traffic as possible into their licensed bands so they can deliver the required levels of voice and data service to the maximum number of subscribers.

In the government and military realm, organizations tasked with monitoring both domestic and overseas radio traffic for sensitive information must constantly upgrade system-loading capacities and develop new strategies to automate the information processing. Advanced radar systems must detect and identify stealthy targets at greater distances and track them with improved accuracy. Airborne countermeasure systems must constantly evolve in complexity to avoid detection.

The only viable solution to all of these problems is Software-Defined Radio. These systems replace traditional analog radio components with FPGAs and other digital signal processing hardware to deliver precise, complex modulation schemes to meet the constantly increasing demands of each application. Meanwhile, the new Xilinx Virtex-7 aims to address the most difficult application challenges in Software-Defined Radio engineering.

Virtex-7 FPGAs: Power, other considerations

The newest generation of FPGAs from Xilinx is the Series 7, consisting of three families each targeting specific price/performance spaces. The Virtex-7 family offers the highest performance of the Xilinx

families with twice the performance of the Virtex-6. Figure 1 shows a comparison of Virtex-6 and Virtex-7, illustrating the performance and other improvements.

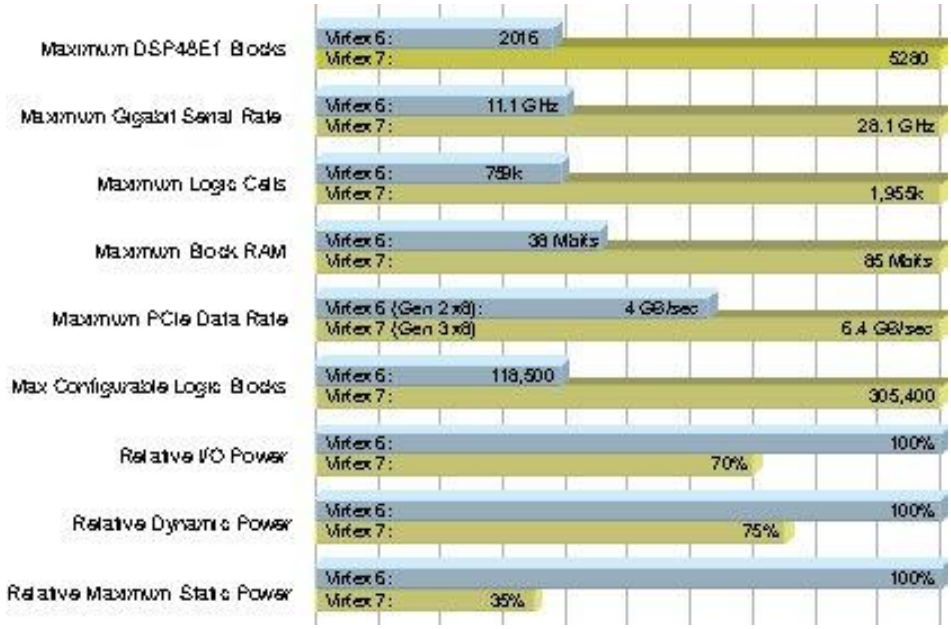

Figure 1: A comparison of Virtex-6 and Virtex-7

Virtex-7 devices feature low-power 28 nm process technology to implement up to 3.1 Tbits/sec of I/O and over 2 million logic cells. They provide up to 6.7 TMACs of DSP resources, especially important for Software-Defined Radio applications. Because of new process technologies and other power management schemes, they consume half the power of Virtex-6 for a given function.

Figure 2 shows the steady improvement in the past four generations of Xilinx FPGAs starting with the Virtex-4 and continuing to the Virtex-7. The graph displays the number of logic cells contained in a range of different density devices in a 35 mm x 35 mm BGA package. This clearly shows the dramatic increase in resource density, bounded by the constraints of the size and power dissipation.

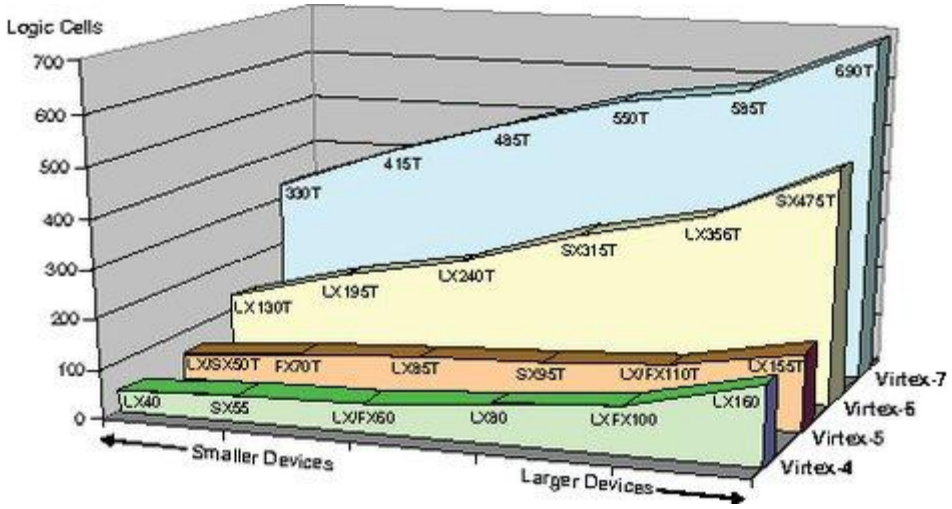

Figure 2: The steady improvement in the last four generations of Xilinx FPGAs, starting with the Virtex-4 and continuing to the Virtex-7.

Challenge No. 1: DSP engine implementation

Software-Defined Radio signal processing algorithms for the new complex modulation waveforms require substantial computational horsepower, which isn't always easy to come by. However, general-purpose processors execute software instructions sequentially on one or more arithmetic units, while FPGAs implement algorithms with numerous DSP hardware engines operating simultaneously in parallel. In this way, FPGAs not only improve algorithm processing speeds for a given channel, but given enough DSP engines, they can handle multiple channels operating in parallel. Because these engines are configured and connected by the designer, FPGAs can be tailored to meet a wide range of different applications to overcome most any design challenge.

Virtex-7 FPGAs use the DSP48E1 engines first introduced in the Virtex-6 family, each containing a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator. The maximum quantity of DSP48E1 engines in Virtex-6 devices was 2016, while the Virtex-7 boosts the maximum count nearly two-and-a-half times to an impressive 5,280.

Challenge No. 2: Data converter interfaces

All Software-Defined Radio systems need A/D and D/A converters in the antenna path. To feed the insatiable demand for wireless data service, new wideband standards like UMTS and LTE can deliver wireless data rates up to 100 Mbps. But these services require advanced modulation schemes and channel bandwidths to 20 MHz and beyond. Advanced radar systems with sophisticated pulse structures call for signal bandwidths of 300 MHz and higher.

Because Software-Defined Radio deals so well with these complex waveforms, one major objective is to process signals as close to the antenna as possible. Fortunately, the latest Virtex-7 FPGAs provide a direct connection to high-speed peripheral devices with LVDS DDR I/O transfer rates reaching 1,600 MHz, up from 1,400 MHz in the Virtex-6. Applications such as a Virtex-7 XMC Software-Defined Radio module can use a 3.6 GHz A/D converter, taking full advantage of the high-speed I/O capabilities of the Virtex-7 FPGA.

To ease onerous printed circuit board layout constraints, Virtex-7 has per-bit skew adjustments to help align bits in a data word. They also include digitally controlled termination networks for tuning optimum performance while eliminating the need for external discrete resistors.

Challenge No. 3: Data buffering

While Software-Defined Radio A/D and D/A converters operate at a constant clock rate, networks and system buses transfer data most efficiently in packets or blocks. This requires staging of data in buffers that are sized to handle the worst-case delay until access is granted to use system memory. As data converter rates increase, buffer memory fills more quickly, shrinking the maximum buffer time and risking the loss of data.

Internal FPGA block RAM can be used as swinging or “ping-pong” memory buffers. Here one buffer fills from the source (like an A/D converter) while the other empties to the destination (like the PCIe interface), with roles reversing each cycle. Another very popular elastic buffer structure is the FIFO.

The largest Virtex-7 devices now offer more than 85 Mb of internal block RAM, more than twice as much as Virtex-6. Nevertheless, internal block RAM can fall short of meeting the required buffer sizes, and external memory must be used.

Challenge No. 4: Those external memory interfaces

Software-Defined Radio applications use large blocks of memory not only for buffering real-time data, but also to support complex signal processing algorithms. Thus, it’s a real problem when data buffers are too small or memory read/write cycles are simply not fast enough.

Synchronous DRAMs offer the densest and most economical solution for large memory arrays. Developed to support high-end PCs, DDR3 SDRAMs deliver extremely fast read/write rates by transferring data on both edges of the clock. The latest Virtex-7 devices can support DDR3 devices running a bit transfer rate up to 1.866 Gbps – far above the 1.066 Gbps for Virtex-6.

To achieve these speeds in the Virtex-7, the maximum 1:2 ratio between the fabric logic clock and the memory transfer rate on the Virtex-6 was boosted to 1:4 on the Virtex-7. Also new on the Virtex-7 is the Phaser clock generator that maintains real-time clock-to-data timing to within 7 psec. Designated interface pins allow a direct, glueless connection to these fast memories.

Challenge No. 5: High-speed interconnections

Since most Software-Defined Radio systems utilize real-time embedded system board-level products, high-speed interconnections such as Gigabit serial links and PCI Express are essential to handle the increased digital traffic between components, boards, and chassis to support new wideband signals. Needless to say, any bottlenecks for such wideband signal traffic will cripple real-time SDR operation.

In their latest Virtex-7 devices, Xilinx offers gigabit serial transceivers with four different maximum bit rates: 6.6 GHz (GTP), 12.5 GHz (GTX), 13.1 GHz (GTH), and 28 GHz (GTZ). This represents a dramatic increase over Virtex-6 maximum serial transceiver rates of 6.6 GHz (GTX) and 11.1 GHz (GTH).

These interfaces support popular protocols such as Ethernet, Aurora, SerialRapidIO, PCIe, and others. At the higher Virtex-7 rates for GTH, each 8x Aurora link can deliver bidirectional transfers up to 10 GBps.

Unlike Virtex-6 devices, some Virtex-7 devices now support the PCI Express Base Specification 3.0 with capabilities for both endpoint and root port. Since each PCIe generation also accommodates lower generation devices, the Gen3 interface operating at 8 Gbps is backward compatible with Gen1 at 2.5 Gbps and Gen2 at 5 Gbps. The x8 Gen3 PCIe interface provides a 6.4 GBps system interface.

Virtex-7 enhances SDR

When coupled with advanced power reduction techniques, more DSP engines for signal processing, improved buffering, and faster interfaces for data converter and memories, it is easy to see how developers can take advantage of the new Virtex-7 FPGAs to implement significant improvements in overall Software-Defined Radio system performance. CS

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