Military

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Virtex-7 FPGA technology boosts radar performance

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The latest Virtex-7 FPGAs from Xilinx deliver significant benefits for radar systems compared to previous-generation devices. Higher-density silicon with lower power consumption, more resources, faster interfaces, and more and faster memory not only enhances performance, it also opens new application spaces.

Since the advent of the first military radar systems more than 80 years ago, engineers have continuously enhanced capabilities and performance levels by harnessing new technology and components. The perpetual leapfrog race between improved detection and better countermeasures offers a steady stream of recurring opportunities for system designers to deploy advanced techniques and algorithms with increasingly higher levels of sophistication.

Because of their inherent reconfigurability and real-time signal processing resources, FPGAs are almost always the critical link for advancing radar technology to the next level. Xilinx's latest generation of FPGAs, the Series 7, consists of three families addressing a range of price and performance markets, the most powerful being the Virtex-7. By using a new 28 nm High Performance Low power (HPL) process technology, the Virtex-7 boasts twice the performance and half the power consumption of its predecessor, the Virtex-6. Figure 1 summarizes relative resource comparisons between the two families, clearly showing dramatic improvements.

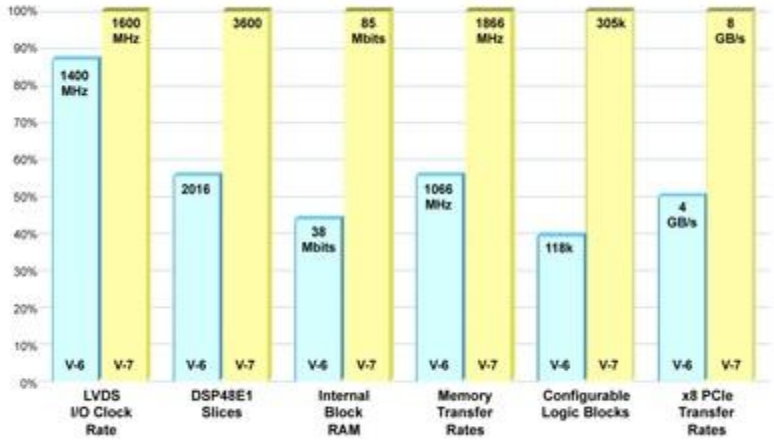

Figure 1: Radar resources comparison between Virtex-6 and Virtex-7

(click graphic to zoom by 1.9x)

Faster peripheral interfaces, more DSP[] engines and block RAM, enhanced memory interfaces, and faster PCIe interfaces in the Virtex-7 all directly impact radar performance. At the same time, power dissipation for a given function has dropped by half compared to previous-generation devices, opening up new applications for smaller unmanned vehicles.

Faster A/D and D/A interfaces

Figure 2 shows a generic block diagram illustrating the basic functions of a typical FPGA[]-based radar receiver. An analog[] RF tuner translates the antenna frequency band of interest down to a lower IF frequency that can be sampled by an A/D converter. Thereafter, all signal processing, control, storage, and system interface functions are handled by the FPGA.

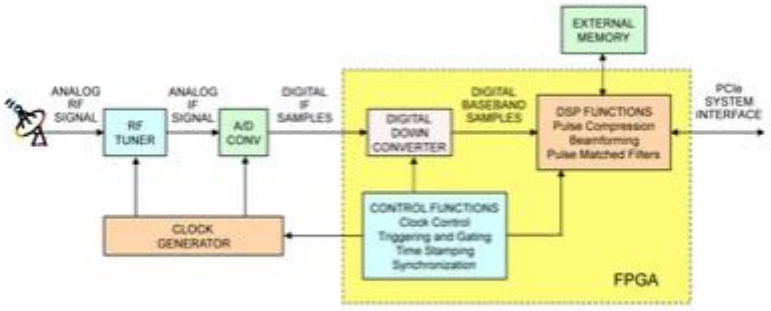

Figure 2: Functional blocks of a typical FPGA-based radar receiver

(click graphic to zoom by 1.9x)

Signal bandwidths in modern radar systems can exceed 500 MHz, pushing the sampling rates for A/D and D/A converters well into the GHz range in some cases. These increasingly higher rates not only challenge interface speeds of FPGAs, but various voltages levels and clocking schemes used in the A/Ds also present special data packing and formatting requirements.

Very high-speed A/D converters demultiplex the output samples onto multiple buses to gain a more manageable bus clock rate. To support them, the Virtex-7 FPGAs offer a direct connection with LVDS DDR I/O transfer rates reaching 1,600 MHz, up from 1,400 MHz in the Virtex-6. Now, for example, a four-way demultiplexed A/D can operate at up to 6.4 MSamples/sec, so it can digitize a wideband radar signal with an instantaneous RF bandwidth approaching 3 GHz.

These new highly configurable Virtex-7 interfaces include per-bit skew adjustments to help align bits in a data word to ease stringent trace length matching in printed circuit board design. Also, digitally controlled termination networks eliminate the need for external discrete impedance-matching resistors to achieve reliable data connections.

The architecture for FPGA-based radar transmitters is analogous, but with inverse signal flow structures including D/A converters, RF upconverters, and power amplifiers. Similar requirements for extremely fast interfaces to wideband D/A converters benefit from the same Virtex-7 speed and configurability improvements discussed.

Enhanced DSP resources for radar

Transmitted radar signals are becoming increasingly sophisticated to improve performance in target range, position and classification, resistance to clutter for

low-altitude targets and weather, and resistance to electronic countermeasures and detection. Outgoing radar pulses must be precisely crafted for amplitude, frequency, and phase, and often these characteristics must change dynamically to adapt to different targets, trajectories, or conditions.

Complex outgoing radar pulses previously required the use of signal synthesis tools to precompute the waveforms, which were stored in memory for D/A playback. FPGA DSP engines can now be harnessed to compute the required transmit waveforms in real time, a major benefit for intelligent, adaptive radar systems.

Different signal processing is required for received radar signals. Some of the more important algorithms are digital downconversion, pulse matched filters and pulse compression, forward and inverse FFTs, windowing, and matrix operations. Before FPGAs took over the job, massive DSP subsystems were required to handle these compute-intensive operations because they had to be computed in real time.

Additionally, one of the most critical DSP operations for radar is beamforming, which governs the operation of phased array antennas, both for transmitting and receiving. By carefully adjusting the relative phase of signals for each antenna element, the antenna array can be electronically steered for maximum signal strength in any direction. The phase shifts are introduced electronically in the transmit and receive paths of each element through DSP operations easily implemented in the FPGA, eliminating the need for cumbersome mechanical structures.

Accordingly, Virtex-7 FPGAs use the same DSP48E1 engines first introduced in the Virtex-6 family, each containing a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator. However, to support all of these increasingly demanding signal processing requirements for complex, wideband radar signals, the quantity of DSP48E1 engines in the Virtex-7 has been boosted to 3,600. This represents an increase of nearly 80 percent more than the largest Virtex-6 device, directly enhancing each of the critical transmit and receive capabilities needed for the latest radars.

Faster and deeper memory

Fast local memory provides an enormous benefit to receive-side signal processing because most radars use range gating to capture the reflected signals during a specific time window relative to the outgoing pulse. The ratio of the range gate interval to the pulse repetition period determines the acquisition duty cycle. By storing the incoming data samples from the A/D converter in real time during the range gate, DSP blocks have more time to complete the signal processing tasks, since no new data will be acquired until the next range gate.

This can dramatically improve the efficiency of the DSP hardware by several times, depending on the duty cycle.

The largest Virtex-7 devices now offer more than 85 Mb of internal block RAM for intensive on-chip DSP operations, more than twice as much as Virtex-6. But transient capture and buffering of large blocks of data require external memory that can keep up with the A/D sample rates.

Synchronous DRAMs deliver extremely fast read/write rates by transferring data on both edges of the clock. They also offer the densest and most economical solution for large memory arrays. The latest Virtex-7 devices can support DDR3 devices running a bit transfer rates up to 1.866 Gbps, far above the 1.066 Gbps for Virtex-6.

The Virtex-7 achieves these speeds by boosting the maximum 1:2 ratio between the fabric logic clock and the memory transfer rate on the Virtex-6 to 1:4 on the Virtex-7. The Virtex-7 also introduces the Phaser clock generator to maintain real-time clock-to-data timing to within 7 psec for direct, glueless connections to these fast memories.

Timing is everything

All radar systems require precise timing between the transmit pulses and the acquisition of the return signals at the receiver. FPGAs abound in configurable logic resources ideal for state machines and counters to create extremely sophisticated timing scenarios for range gating and adaptive algorithms to maximize target tracking and identification. Coupled with agile beamforming capabilities, FPGAs can implement multiple target tracking algorithms using a single fixed array.

The number of available configurable logic blocks in the largest Virtex-7 device is 305,400, compared to the Virtex-6 maximum quantity of 118,500. This 2.5-fold increase can also be taken advantage of to implement new features such as GPS receiver time stamping of received radar pulses to capture not only the precise acquisition time, but also geographic coordinates.

Zero bottleneck system interface

A fast system interface ensures no data bottlenecks for wideband radar signals on the path to or from a downstage processor or storage facility. Because PCIe has become a de facto industry standard interface solution for embedded system boards, Xilinx includes silicon PCIe interface blocks incorporating the key layers of the PCIe protocol stack and fast gigabit serial transceivers.

The Virtex-6 PCIe interface accommodates PCIe Gen 2 x8, delivering a peak rate of 4 GBps using a 5 GHz bit clock and 8B10B encoding on each of the eight

bidirectional lanes. With faster transceivers and enhanced circuitry, the Virtex-7 uses an 8 MHz bit clock and 64/66 channel coding to support PCIe Gen 3 x8, delivering a peak transfer rate of 8 GBps, doubling throughput to the system.

Virtex-7 scores high marks for radar

Virtex-7 delivers key improvements in peripheral speed, DSP resources, internal and external memory size and speed, logic resources, and PCIe system interfaces, while at the same time dropping power consumption. Again, the perpetual leapfrog race in radar between improved detection and better countermeasures offers significant new opportunities for system engineers to take advantage of each of these new features. An example is Pentek's Virtex-7 XMC module, targeting wideband radar applications with three 200 MHz 16-bit A/Ds, two 800 MHz 16-bit D/As, and 4 GB of SDRAM. It takes advantage of all of the resources discussed and represents a quantum step in performance over earlier Virtex-6 products. MES

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