

# The Pentek Pipeline

*A quarterly publication for engineering system design and applications.*

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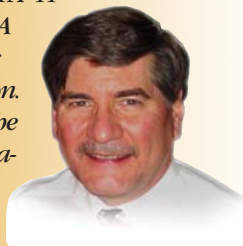
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**In This Issue**

- The recent adoption of gigabit serial interfaces represents the biggest performance leap for the VMEbus since its introduction. More about it in the feature article.

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*Rodger Hosking, Pentek Vice President and Co-founder*

- **Product Focus:** Model 4207 VXS I/O Processor with dual PMC/XMC sites [Click here](#)
- **Webcast:** for a 10-minute Model 4207 overview [Click here](#)

**Technical Resources**

*New!* Download the 1st edition of the *High-Speed Switched Serial Fabrics Handbook:*

[pentek.com/go/pipescrhb](http://pentek.com/go/pipescrhb)

Download the 6th edition of the *Digital Receiver Handbook:*

[pentek.com/go/pipedrhb](http://pentek.com/go/pipedrhb)

Download the 3rd edition of *FPGAs for Software Radio Handbook:*

[pentek.com/go/pipefpghb](http://pentek.com/go/pipefpghb)

Download the 2nd edition of *Critical Techniques for High-Speed A/D Converters in Real-Time Systems*

[pentek.com/go/pipehshb](http://pentek.com/go/pipehshb)

**System-level Switched Topologies for Extreme Performance**

Through evolutionary enhancements and technology developments, VMEbus still serves as the dominant bus structure for high-performance, real-time embedded systems. When VMEbus was first introduced, interboard transfer rates of 30 or 40 MBytes/sec of its shared bus backplane was more than adequate for most applications.

As requirements grew, VME acquired new interfaces such as VSB, RACEway, RACE++, VME64, VME320, and 2eSST, thereby ensuring a healthy community of suppliers and a new stream of backward-compatible products. This continues to be very important to risk-averse government agencies selecting products for long-term programs that require support and maintenance for a dozen years or more.

Well into its third decade of widespread deployment, the recent adoption of gigabit serial interfaces for VME clearly represents the most significant leap of performance throughout its entire history.

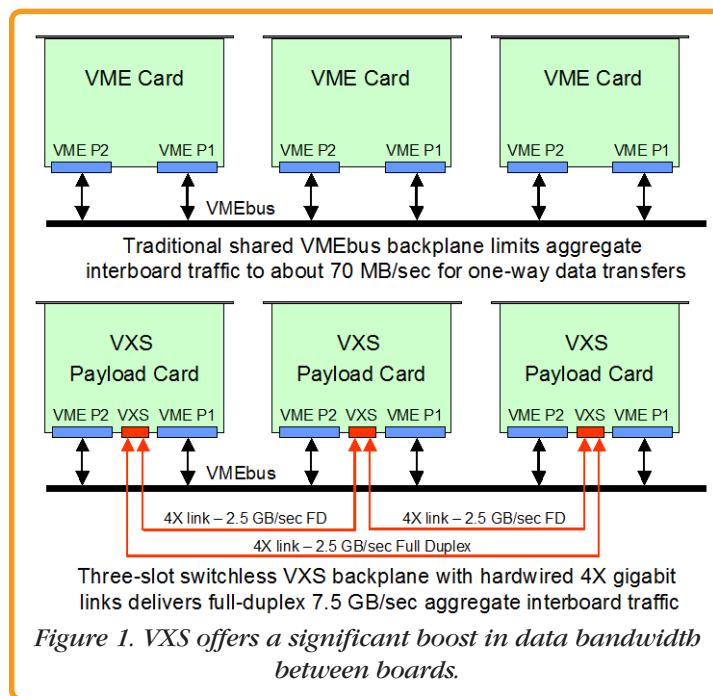
**VXS: Switched Fabric for VME**

Motorola’s VME Renaissance announcement in 2003 unveiled a new standard called VXS, officially designated VITA 41 by the VITA standards organi-

zation. It defines the implementation of gigabit serial technology for VME in a logically layered specification, while carefully preserving the legacy VMEbus form factors and bus operations. At the top layer, VITA 41.0 defines the connectors, pin designations, dimensions and mechanical structures for cards and backplanes—completely free of any mandates for specific protocols or fabrics.

One of the biggest challenges was the choice of a suitable connector that could handle serial signals at bit rates up to 10 GHz, while not interfering with existing mechanical structures such as legacy VME P1 and P2 connectors and PMC modules. It also had to be readily available from one or more vendors at a reasonable price. The solution was Tyco’s MultiGig RT2 connector supporting sixteen differential gigabit signal pairs and four single-ended signals. The sixteen pairs are usually ganged into two 4X links, each with four transmit and four receive signals. Each link forms a full duplex channel capable of delivering data at 1.25 GBytes/sec in both directions simultaneously when operating at bit rates of 3.125 GHz on each serial lane.

VXS defines two types of cards: the Payload Card and the Switch Card. Both utilize the same



mechanical outline as a standard 6U VMEbus card. The payload card fits the new MultiGig RT2 connector in between the existing P1 and P2 connectors in a position designated P0. Most legacy VME backplanes provide clearance for the new P0 connector, thus allowing insertion of VXS cards for backwards compatibility even though the VXS interface is not engaged.

VXS backplanes have one mating MultiGig RT2 connector for each payload card slot. VITA 41 does not dictate any specific backplane topology and leaves plenty of flexibility for various architectures. The simplest configuration is the VXS switchless mesh backplane shown at the bottom of Figure 1. ➤

## System-level Switched Topologies for Extreme Performance

► Here, three VXS cards are joined in a ring configuration, with each card connected to the other two through two 4X links hard-wired in copper as part of the backplane design. At a serial bit rate of 3.125 GHz, this system supports simultaneous data transfers between the cards in both directions at an aggregate rate of 7.5 GBytes/sec.

As a comparison, a traditional three-card VMEbus system shown at the top of Figure 1 shares a common backplane bus that allows one data transfer in one direction at a time. At rates of up to only about 70 MBytes/sec, it is more than two orders of magnitude slower than its VXS counterpart in Figure 1.

VXS also defines an alternative backplane topology that uses a switch card to join cards using the 4X serial links. Although the switch card still retains the VME 6U form factor, it differs from the payload card in that it does not have P1 and P2 connectors. In their place are additional MultiGig RT2 connectors offering as many as 22 serial 4X links to the backplane for connection to multiple payload cards and other switch cards.

“transparent” to the serial traffic protocol, where the switch ports are assigned by some other method, such as an on board controller receiving commands over an Ethernet link.

In either case, unlike the dedicated paths of the switchless backplane, the switch card topology offers excellent flexibility in assigning a data flow within the system. This can be a static data flow pattern established during initialization or dynamic routing during runtime. For high-reliability applications, two switch cards provide redundancy because payload cards can be joined through either switch.

Maximum data transfer rates in this switched star VXS system are 2.5 GBytes/sec in each direction for each payload slot, for a full-duplex aggregate rate of 100 GBytes/sec for a 21-slot system!

Figure 2 also shows another key extension to VXS: gigabit Ethernet control plane links. Apart from the dual 4X data links, each payload MultiGig connector also supports two 1X GigE-X ports, each using two differential pairs, one for each direction. Multiple GigE-X ports from the payload cards are sent to one of the MultiGig con-

### VXS Extensions

Many extensions to the base VITA 41.0 specification are now released or in working groups at VITA. These extensions are defined by sub-specifications, like the GigE-X control plane now being developed under VITA 41.6. Most of the other extensions implement various switched fabric standards over the 4X data plane links on VXS including Infiniband (41.1), Serial RapidIO (41.2), Gigabit Ethernet (41.3), PCI Express (41.4) and Xilinx Aurora (41.5).

A follow-on standard being defined under VITA 46 draft specification, also known as VPX, extends the number of MultiGig RT2 connectors on the payload cards by completely eliminating the P1 and P2 connectors. As a result, VPX payload cards support a much higher traffic bandwidth than VXS payload cards. Like the VXS specifications, VPX also has sub-specifications for several fabric protocols and other enhancements.

### VXS Products

In the five years since its introduction, dozens of embedded computer hardware vendors have developed hundreds of VXS products. They include switchless mesh backplanes, switched star backplanes, complete card cages and chassis, switch cards, A/D and D/A converters, software radio cards, PMC and XMC carriers, single board computers, DSP and RISC array processors, FPGA cards, memory cards, as well as copper and optical LAN, WAN and disk storage adapters.

VXS fully supports PMC mezzanine modules, allowing systems integrators to take advantage of that enormous base of existing I/O products available prior to VXS.

Concurrent with the introduction of VXS, the gigabit serial extension to PMC known as XMC was introduced and later defined under VITA 42. XMC modules connect to the VXS carrier card with two or four 4X links, supporting transfer rates up to 5 GBytes/sec and eliminating the legacy PCI bus bottleneck. ►

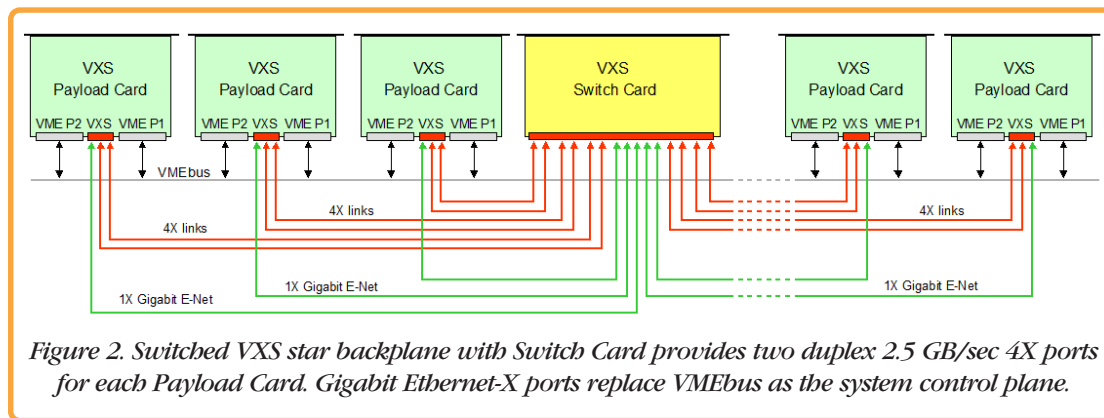


Figure 2. Switched VXS star backplane with Switch Card provides two duplex 2.5 GB/sec 4X ports for each Payload Card. Gigabit Ethernet-X ports replace VMEbus as the system control plane.

Figure 2 shows a typical “star” topology backplane with two 4X links from each payload card hard-wired to one switch card. Each payload card can connect to any two other payload cards according to the routing paths provided by the switch card. The switch card can be dedicated to a particular serial protocol, which determines the switch path routing through inspection of packet header routing information. Alternatively, the switch card can be

dedicated to a particular serial protocol, where they are connected with an Ethernet switch or hub. By allowing Ethernet commands to be passed between boards, these GigE-X ports are intended to replace the control plane function of the VMEbus. With this elegant, high-performance solution for both data and control planes, the VXS standard opens up a new range of system applications previously unattainable.

## System-level Switched Topologies for Extreme Performance

➤ As an example, Figure 3 shows the recently introduced Pentek Model 4207 VXS PowerPC I/O processor with dual XMC sites and a wealth of critical interfaces for high-performance embedded systems. At its heart is an on-board fabric-transparent gigabit serial crossbar switch, highlighting the vital role of serial technology for interconnecting resources within the board and to other boards across the backplane.

### VXS System Example

Taking advantage of the tremendous bandwidth afforded by VXS, the 16-channel beamforming signal processor and recording system shown in Figure 4 digitizes 16 antenna IF inputs using four 4-channel A/D converter Pentek 7142 XMC modules. Installed FPGA IP cores on the XMC modules perform digital downconversion from IF to baseband producing four 15 MHz baseband signals, each requiring a data transfer rate of 75 MBytes/sec, or 300 MBytes/sec for each XMC.

Serving as a dual XMC carrier, the Model 4207 delivers data from the two XMC modules over one 4X VXS link across the backplane to the VXS switch card at 600 MBytes/sec. A second identical 8-channel subsystem completes the front-end functions of digitizing and delivering data for all 16 channels.

Data streams from each 4207 subsystem are alternately delivered through the switch card into one 4X port of a DSP VXS card where the beamforming signal processing algorithms are performed. After processing, the 1200 MByte/sec input data stream is reduced to 600 MBytes/sec and delivered over the second 4X port, through the switch card, into a third 4207 on the right. Here, the data is buffered in memory, formatted into a Fibre Channel stream and then delivered to a Fibre Channel disk array for real time storage.

Aggregate bandwidth within this five-slot VXS system is 3.6 GBytes/sec, far exceeding traditional VMEbus capability, yet comfortably below the 10 GByte/sec limit for this VXS configuration.

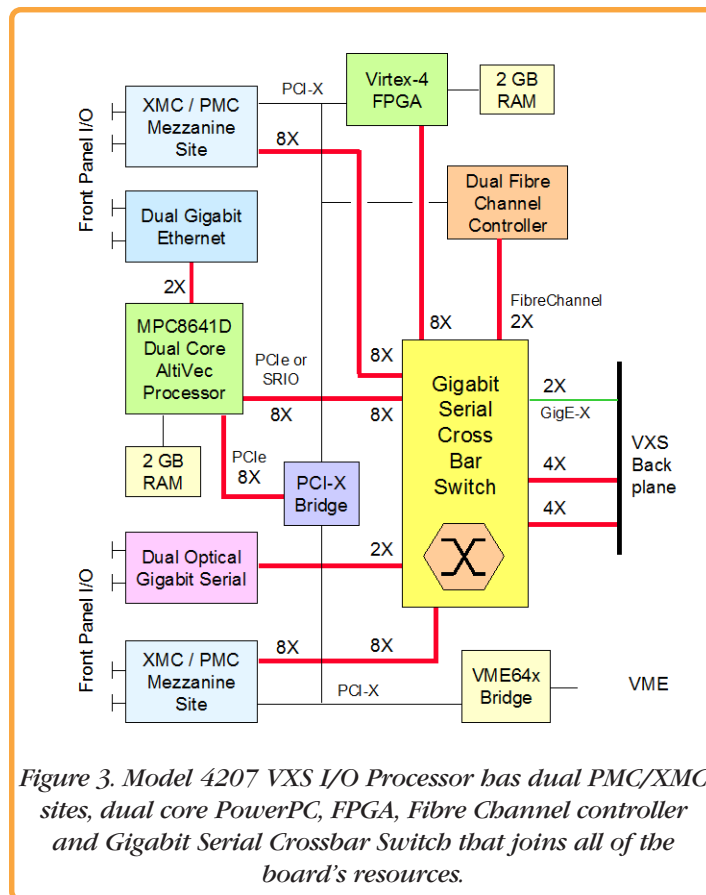


Figure 3. Model 4207 VXS I/O Processor has dual PMC/XMC sites, dual core PowerPC, FPGA, Fibre Channel controller and Gigabit Serial Crossbar Switch that joins all of the board's resources.



### VXS or VPX?

While VPX can deliver much higher aggregate transfer speeds than VXS, a vast majority of system requirements, such as the one shown in Figure 4, can be fully satisfied by the tremendous boost in rates that VXS offers over the legacy VMEbus. Compared to VPX, VXS offers lower costs and is compatible with the thousands of VME boards available from an active community of COTS vendors. With so many VXS products available today and with the VPX standardization still underway, system integrators can be well served by selecting VXS architectures for

today's high performance applications. Investments made by board vendors and system integrators in VXS hardware, interfaces, middleware, software and applications will translate easily into VPX, when system needs dictate. For all of these very tangible considerations, VXS and VPX will likely co-exist for many years to come. □

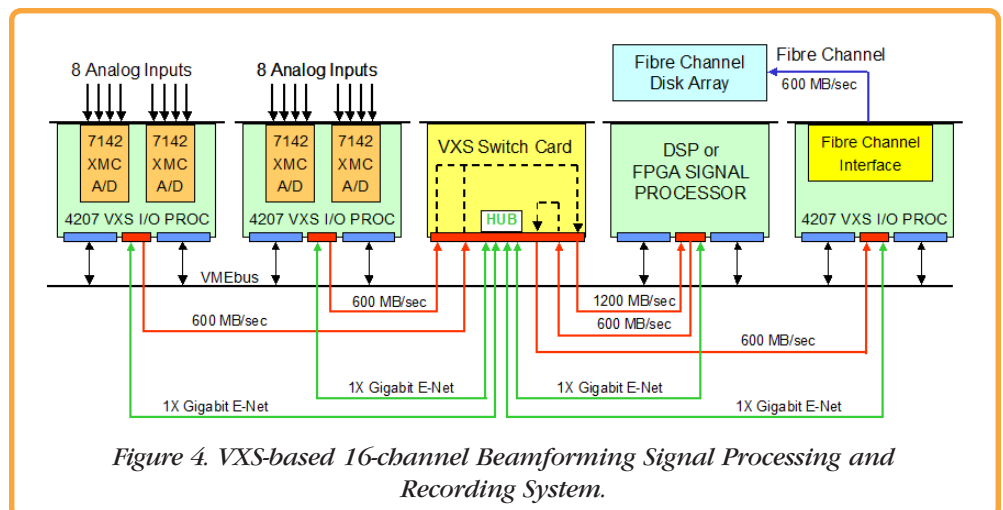


Figure 4. VXS-based 16-channel Beamforming Signal Processing and Recording System.

# Product Focus

## Model 4207

## VME/VXS I/O Processor with two PMC/XMC Sites, Dual Core PowerPC, FPGA and Extreme Connectivity

### General Information

The Pentek Model 4207 PowerPC® VME/VXS I/O Processor board targets embedded applications that require high performance I/O and processing. With two PMC/XMC module sites, the 4207 offers powerful one-slot solutions with nearly unlimited high-speed connectivity.

### Uniquely Designed for Connectivity

Utilizing a unique crossbar switch architecture, the 4207 allows you to make the connections you want between board resources and high-speed interfaces. You don't need hard-wiring or FPGA space to define your I/O data flow and resource assignment. The 4207 supports numerous interfaces including VME64x, gigabit Ethernet, RS-232 and, optionally, dual 4-Gbit Fibre Channel. All interfaces can be included without exceeding the one-slot configuration.

### The Processing Power You Need

The Freescale® MPC8641 utilizes the AltiVec® engine to perform parallel processing of multiple data elements (SIMD) with 128-bit operations. The AltiVec processor executes both fixed- and floating-point instructions. It is available with either a single or dual e600 PowerPC core with maximum clock frequency of 1.5 GHz.

### Zero Latency Crossbar Switch

The 4207 features a zero-latency high-speed crossbar switch architecture that bridges the various board interfaces and resources via gigabit serial data paths. Programmable input equalization and output preemphasis enable optimization for each application. Gigabit serial paths include links to the processor that can be used for 8X PCI Express or 4X Serial RapidIO.

Other gigabit paths, not restricted to any protocol, include two 4X links to each XMC module site, two 4X links (or four 2X links) to the FPGA RocketIO ports, and another pair of 4X links to the optional P0-VXS connector. The switch also provides high-speed connectivity to the optional Fibre Channel controller and front panel optical gigabit serial interface.

### Features

- Freescale MPC8641 single or dual core
- Hosts two PMC or XMC modules
- Virtex-4 FX Series FPGA
- Two gigabit Ethernet interfaces
- Two 64-bit PCI-X buses
- Up to 4 GB DDR2 SDRAM
- VME64x master/slave interface
- Optional 4-Gbit dual optical Fibre Channel controller
- Optional dual optical gigabit serial/ Fibre Channel interface
- Optional VXS interface
- Ruggedized and conduction-cooled versions



### ► PMC/XMC Mezzanine Sites

Model 4207 includes two 64-bit PMC module sites which accept industry-standard modules up to 133 MHz for a wide variety of functions. The PMC modules are accessible from the MPC8641 processor and the VMEbus. A PCI bridge at each PMC site allows operation of slower 33 or 66 MHz modules while running the attached PCI-X bus at a higher speed.

The 4207 PMC sites are also equipped to accept XMC (switched-fabric PMC) modules. Gigabit switched-fabric connectors are optionally provided to support two 4X full-duplex serial ports. Each port allows high-speed data transfer to the crossbar switch using gigabit fabrics such as Xilinx Aurora, serial RapidIO, or PCI Express.

### FPGAs to Suit Your Application

The 4207 may be optionally equipped with a Xilinx Virtex-4 FX FPGA, either the XC4VFX60 or the XC4VFX100. The FPGA is optionally equipped with 1 GB or 2 GB of DDR2 SDRAM memory along with 128 MB FLASH. Two 4X RocketIO ports provide a high-speed serial data path to and from the FPGA. These ports can also be configured as four 2X paths.

Unused FPGA resources are available for the user to implement custom signal-processing configurations and algorithms using Pentek's GateFlow® FPGA Design Kit and the high-performance IP Core Library.

### Local Memory

The MPC8641 is equipped with 1 MB on-chip L2 cache per processor core. 1 GB or 2 GB DDR2 SDRAM is also provided for program and data memory, along with a nonvolatile 128 MB FLASH memory for initialization, self-test and boot code.

### Two PCI-X Buses

The Model 4207 architecture includes two 64-bit PCI-X buses. PCI-X bus 0 provides access to the VMEbus and its associated PMC/XMC mezzanine site. PCI-X bus 1 provides access to its associated PMC/XMC mezzanine site and the optional dual Fibre Channel interfaces.

### Dual Fibre Channel Interface

The 4207 features an optional dual Fibre Channel controller with optical front panel interface for high-speed data transfer to and from Fibre Channel storage devices. When installed, both optical interfaces are ►

► located on the 4207 front panel, along with the dual 10/100/1000Base-T Ethernet and the quad RS-232 interfaces. This maintains a single VMEbus slot configuration and allows Fibre Channel data transfer without sacrificing a PMC/XMC site.

### VXS Interface

The 4207 provides two optional 4X full-duplex VITA-41 VXS links to the P0-VXS connector, each capable of peak rates up to 1.25 GB/sec. Each link is attached to the crossbar switch that's compatible with gigabit fabrics such as Xilinx Aurora, Serial RapidIO, and PCI Express. The P0-VXS connector also features a dual 1000Base-X Ethernet interface per the VITA 41.6 draft standard.

### World-Class Software Support

The Model 4207 is supported by world-class software for initialization, control and optimization.

Pentek **VxWorks®** BSPs provide software developers with a complete library of hardware initialization, control and application functions. Used in conjunction with Wind River's **Workbench** software development environment, it speeds application development.

Pentek **Linux** BSPs provide software developers with a complete open-source library of hardware initialization, control and application functions to be used in a real-time Linux operating environment.

Pentek **GateFlow®** Design Kits allow the onboard FPGA to be configured by the user for implementation of custom preprocessing functions. The kit is used in conjunction with the Xilinx ISE *Foundation™* design tools.

Verari Systems' **VSI/Pro** is an implementation of VSIPL scientific and engineering functions optimized for the PowerPC.



## Specifications

### Processor Resources

**Processor:** Freescale MPC8641 (Single Core) or MPC8641D (Dual Core)

**Processor clock:** 1.33 GHz; contact factory for options from 1 - 1.5 GHz

**Level 2 cache:** 1 MB for MPC8641, 2MB for MPC8641D

**DDR2 SDRAM:** 1 GB or 2 GB (optional, one or two 1 GB banks, each 64 bits wide)

**FLASH:** 256 MB, 16 bits wide

**Node Control:** Built into MPC8641

### Mezzanines

Two PMC/XMC sites

### Optional FPGA

**Type:** Xilinx Virtex-4 Series (-11 speed) XC4VFX60 or FX100

**DDR2 SDRAM:** 1 GB or 2 GB (optional, one or two 1 GB banks, each 64 bits wide)

**FLASH:** 128 MB, 16 bits wide (optional)

### PCI-X Bus #0

**Width:** 64 bits,

**Speed:** 100 MHz

### PCI-X Bus #1

**Width:** 64 bits,

**Speed:** 100 MHz

### Global Resources

**VME64x:** Tundra Tsi148 master/slave, slot 1 controller, D64, A32

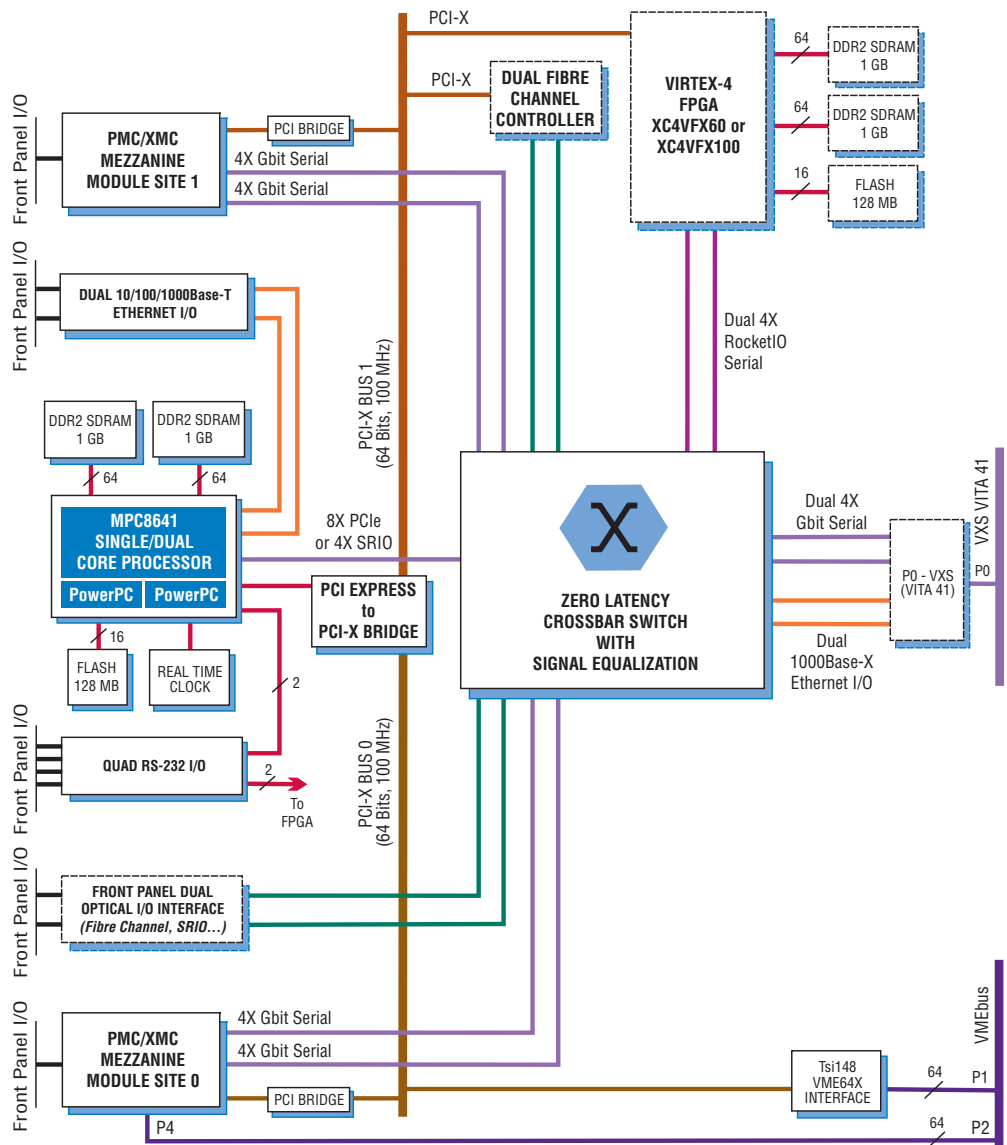
**Serial I/O:** Four RS232 front panel ports

**Ethernet:** Two 10/100/1000Base-T front panel ports, two 1000Base-X ports on rear P0-VXS connector

### Optional Fibre Channel Controller:

Dual Optical, 4 Gbit

**Size:** standard 6U VMEbus board, single slot; board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 0.8 in. wide



For more information and a price quotation go to: [pentek.com/go/pipe4207](http://pentek.com/go/pipe4207)