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Managing New Trends for Embedded EW Systems

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IN THIS ISSUE

Introduction

Electronic Warfare (EW) not only plays a dominant role in worldwide defense capabilities, it also must evolve rapidly to counter new threats and take advantage of new technology. Each advance must take into account the ever-changing system design landscape.

Many critical sections of EW systems are now combined within single components like the RFSoC, including signal acquisition, processing, and generation functions. Increasing complexity in hardware, firmware, and software adds risk and costs, so effective, high-level development tools are becoming more important than ever before.

At the same time, emerging DoD initiatives like SOSA seek to standardize embedded system architectures for improved interoperability and upgradeability, while reducing costs and delivery times. This article discusses new requirements impacting EW system design, and new technologies to help systems integrators succeed.

Scope of Electronic Warfare

EW has evolved to become a dominant military force, often overshadowing the importance of traditional weapons, manpower, and transport systems. EW encompasses an incredibly diverse range of specific military capabilities, each one focusing on widely different aspects of exploiting the electromagnetic spectrum to gain advantage over the enemy. EW signals extend across nearly a dozen orders of magnitude of both frequency and power levels, using a vast array of different platforms for each application.

Deployed EW systems can be found everywhere, including land, air, sea, underwater, and space. They often use the same increasingly-congested slices of the spectrum as non-military radio ➤

activities including commercial, entertainment, government, consumer, municipal, emergency, and transportation purposes. Indeed, our electromagnetic spectrum is a finite resource that is carefully controlled, highly congested, and therefore, heavily exploited by advanced technology to make the most of it.

EW is roughly divided into three major sectors. Electronic Attack (EA) includes classic offensive goals to disrupt, deny, degrade, destroy, or deceive. Electronic Protection (EP) seeks to thwart the effectiveness of EA. Electronic Support (ES) harvests the extensive wealth of signal information of all types to improve decision making and strategies.

EW Challenges and Strategies

Radar represents a major segment of EW, rich with aspects of attack, protection, and support. Under development for nearly a century, radar technology provides critical support for virtually all military platforms. Jamming is one form of Electronic Attack used to destroy, disable, or degrade radar receivers, blinding them to enemy assets. Originally using brute-force, high-power broadband transmitters, jamming has now become extremely sophisticated with highly-directed, frequency- and pulse-adaptive signals. This makes it harder to locate and disable the jamming source.

For Electronic Protection, clever radar transponders in aircraft can generate artificial reflected signals carefully crafted to simulate multiple targets, as well as false location, bearing, speed, and target cross-section information. Short reaction times to synthesize these deceptive signals are vital for air-to-air combat because of close proximities.

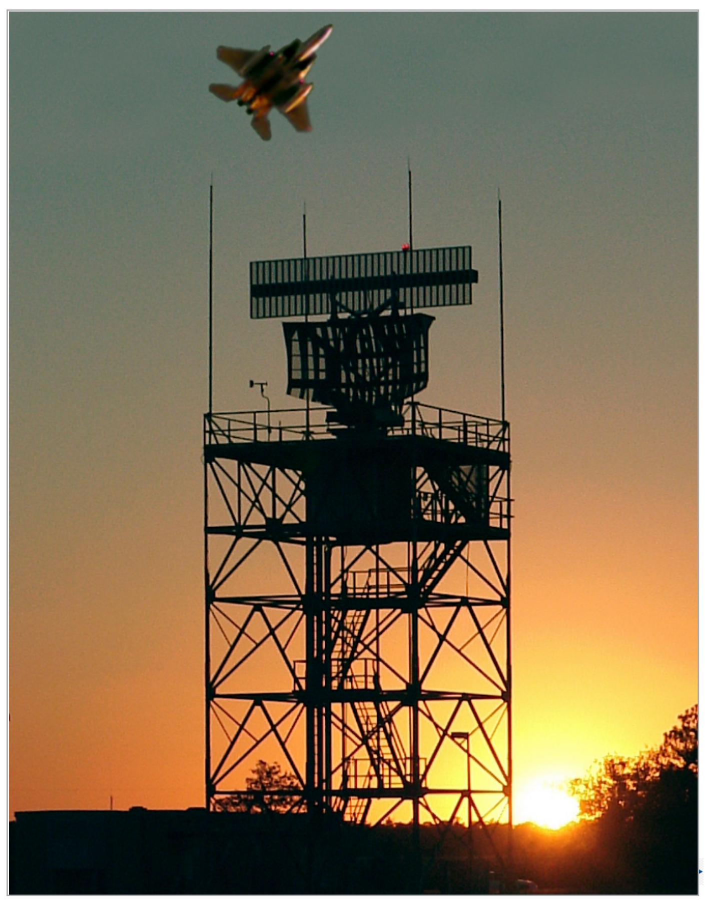
After nearly 25 years, network-centric warfare has evolved rapidly to embrace network technology as a fast, reliable mesh of information links among all warfighting elements. By carefully acquiring signals from radar, communication, electro-optical, and other sensors, and feeding those digitized streams to signal processing elements, algorithms can produce real-time representations of the battlefield for tactical and strategic decisions. Such Electronic Support functions are now greatly enhanced with artificial intelligence and machine learning technologies. Resulting orders containing precise information for the next course of action, carefully tailored for each asset, are distributed quickly across the battlefield network to men and equipment.

These examples illustrate how EW functions for EA, EP, and ES are often highly integrated and interactive within the same platform. All of these operations increasingly rely upon advanced antennas, including phased array designs, and sophisticated signal processing techniques like beamforming, modulation/ demodulation, artificial intelligence (AI), multi-dimensional algorithms, spread spectrum techniques, cryptography, adaptive radio, and cognitive radio.

Nevertheless, any single implementation of these strategies will eventually become less effective as new countermeasures are deployed. This self-sustaining cycle is the engine of EW, which virtually guarantees on-going military funding and incentives for new development.

New Technologies for EW

To advance EW objectives, several critical technologies are required. Many EW signals now occupy wider bandwidths, not only to simply accommodate higher information rates, but also to support spread-spectrum modulation schemes to improve channel reliability and resiliency against jamming. Another contributor is frequency hopping, where RF carrier frequencies are rapidly changed during transmission in a predetermined pseudo-random pattern known only to the receiving device. ➤



This increase in signal bandwidth means wideband analog front end RF and IF circuits, higher sampling rates for the data converters, and increased data rates for digitized signal interface links. Perhaps the biggest effect is the major impact on the workload for digital signal processing engines, which must now implement AI and other advanced, compute-intensive algorithms.

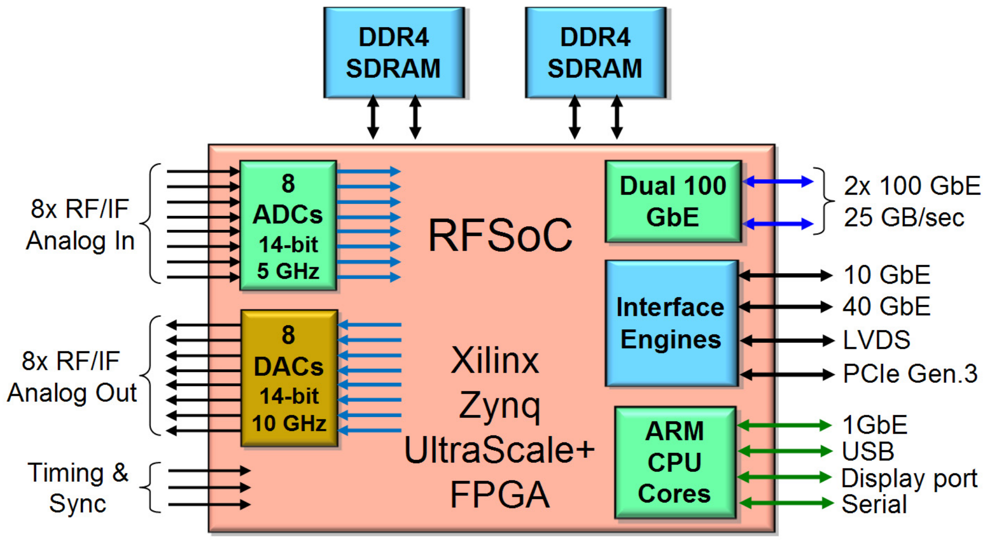


Figure 1: Xilinx's Zynq UltraScale+ RFSoC device combines all critical components of the EW sub-system, including eight RF ADCs and DACs, high-speed Ethernet and PCIe, DDR4 SDRAM interfaces, and multi-core ARM processors.

Phased-array antennas are linear or two-dimensional planar arrays of elements, each one capable of applying independent phase shifts to a common transmit or receive signal. By precisely controlling each phase shift to achieve constructive interference, the antenna can be highly directional, both for receive and transmit. Unlike traditional dish antennas, by applying a new set of phase shifts, phased arrays can be instantly steered to a new direction with no moving parts. Additional signal processing allows simultaneous tracking of multiple targets.

Phased arrays are particularly appropriate for airborne and UAV radars where they can be installed on a hull surface and quickly adapt to threats and targets without the bulky mechanical structures required for a directional dish. But, the agility and reliability of phased arrays makes them increasingly popular for ground- and maritime-based radars as well, especially for fire-control systems and countermeasures.

All of these important benefits incur some complexity and cost. Each element of the phased array requires independent phase-shifts (weights). Originally done with analog circuitry, now this is performed on the digitized signals using DSP because of improved precision and speed. Thus, each element in a transceiver array requires its own ADC and DAC, plus its own DSP engine.

To make this more manageable, the RFSoC (RF System-on-Chip) was introduced by Xilinx in 2017 (see **Figure 1**). Based on its UltraScale+ FPGA Zynq architecture, the RFSoC includes eight ADCs sampling at 5 GS/sec and eight DACs sampling at 10 GS/sec. These are connected directly to the Zynq FPGA fabric, eliminating the power, connections, complexity, and latencies of external interfaces to discrete data converters. An on-board, multi-core ARM processor acts as a system controller with control/status I/O, and two 100 GbE interfaces connect the RFSoC to external devices supporting 25 GB/sec data transfers in both directions.

Introduced for commercial 5G wireless markets, the RFSoC nicely integrates the key support functions for 8-elements of a phased-array antenna, and is small enough to fit right behind the phased array panel to reduce cumbersome cabling. By harvesting this new technology like RFSoC from commercial markets for military applications, defense vendors are dramatically shrinking SWaP and cost, especially critical for air vehicles and small EW countermeasure systems.

Because RFSoC offers a complete software radio sub-system on a chip, it opens open a wealth of new military uses previously impractical with earlier technology. These include small standalone monitoring stations, more capable robots, smarter munitions, and portable adaptive radios that can dynamically change operational frequencies to avoid crowded bands or countermeasures.

New Development Tools for EW

Emerging EW threats and strategies now require exploitation of advanced vector processing, configurable hardware for sensor interfaces, artificial intelligence, neural networks, machine learning, and scalar processing for analysis and decision making. Each of these disciplines currently requires specific processing hardware and specialists who are capable of programming them. Even if each section is fully operational, integrating these diverse resources into a tightly-coupled, functional system is daunting.

Some new initiatives offer a promising path forward. Xilinx recently announced its Versal ACAP (Adaptive Compute

Acceleration Platform) family of hardware devices and supporting development tools. Different members of the family provide different blends of three major resources: scalar processors (CPUs), vector processors (GPUs, DSPs) and adaptable logic (FPGAs). One even offers RF ADCs and DACs, similar to the RFSoC and, therefore, highly appropriate for embedded EW. On-board, high-bandwidth memory and flexible memory structures eliminate the need for external devices. To interconnect these resources, ACAP includes an extremely wideband network-on-chip that offers a uniform interface and protocol to simplify system integration.

Versal development tools target high-level design entry from frameworks, models, C-language, and RTL coding. Users can create a custom development environment to suit their project needs and programming preferences.

Other hardware/software platforms will evolve to help speed EW development tasks to help overcome high complexity and extreme performance requirements.

SOSA - A New Embedded Open Standard for EW

In May 2013, the U.S. DoD issued a milestone memo mandating that all acquisition activity must incorporate DoD Open Systems Architecture (OSA) principles and practices defined in evolving open standards for well-defined modular hardware and software components. The objectives include multi-vendor sourcing, reusability for quick-reaction needs, and easier upgrades to new technology, reducing development risks and ensuring significantly longer operational life-cycles.

In response, each of the three primary U.S. service branches (Army, Navy, and Air Force), began developing standards that embraced OSA principles to meet future procurement needs of deployed systems for their respective services. Five years later, it was apparent that the three services had many common elements, inspiring the formation of the SOSA (Sensor Open Systems Architecture) Consortium to unify these initiatives (see **Figure 2**).

SOSA adopts the most appropriate subsets of existing open standards to form a multipurpose backbone of building blocks for current and future embedded systems for Radar, EO/IR, SIGINT, EW, and communications. SOSA contributing members are U.S. government organizations including the U.S. DoD, Army, Navy, and Air Force, as well as key representatives from industry and universities.

A major SOSA product is the Technical Standard, which draws primarily from OpenVPX and other related VITA standards, plus emerging extensions for new technologies, topologies, and environmental requirements. Now under intensive development for several years, the Technical Standard Snapshot 3 was released in July 2020 for review and amendment

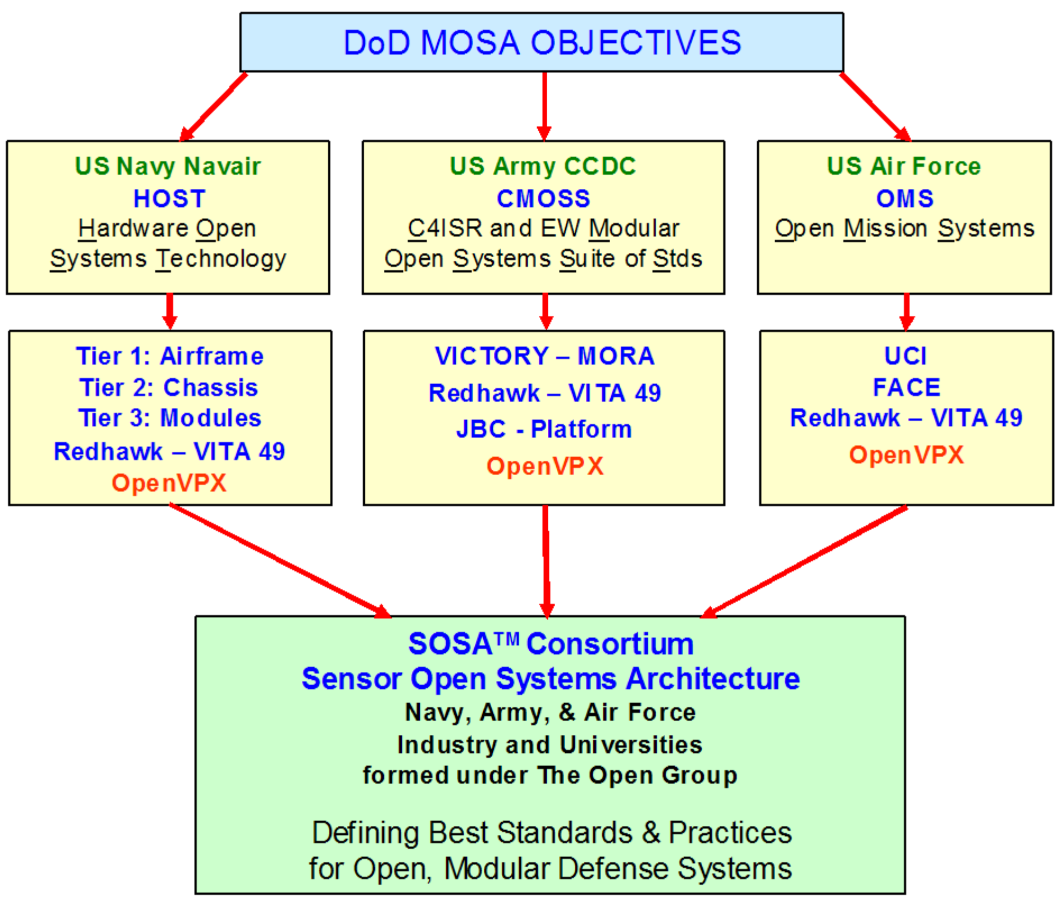


Figure 2: Open Systems Architecture initiatives developed independently by the three U.S. DoD services share common elements that are now consolidated under the Open Group SOSA initiative for open embedded system acquisition requirements.

prior to the first full release at version 1.0 expected in early 2021.

Dozens of vendors are now offering "SOSA-aligned" products that are well poised to become "SOSA Certified" after third-party certification to the final standard once released (see **Figure 3**).

The DoD is now issuing requests for proposals and information clearly favoring respondents that offer OSA-based solutions. A key difference in the SOSA architecture from earlier open standards is the well-defined protection of IP, which encourages innovation and investment. This helps ensure that SOSA is well on its way to revolutionize the future of embedded military EW systems. ☐

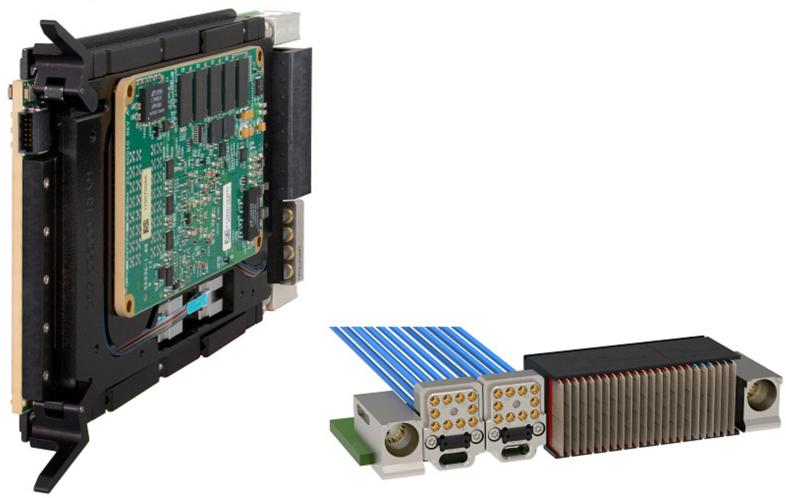


Figure 3: Pentek's **Model 5550 SOSA-Aligned 3U VPX RFSoC Processor Card** with the QuartzXM module on its conduction-cooled carrier, and dual VITA 67.3 rear-panel connectors for 20 RF coaxial cables and dual 100 GbE optical cables.

Military & Aerospace Electronics®

SOSA Draft Industry Standard Picking Up Steam, and May Lead to Official Open-Systems Standard in Early 2021

The emerging SOSA standard aims to enable military embedded systems designers to create new systems and make significant upgrades to existing systems much quicker than today's technologies allow.

Click **here** to read the article.

Focus On: SOSA

Click here to download eBook.

The Evolution of SOSA

Tech Briefs Media Group recently presented a 60-minute webinar that provides a helpful overview of how far SOSA has come to date and where it's going in the future.

Click **here** to access the webinar.

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RFSoC Enabling Radar/Electronic Warfare Systems

The insatiable need for bandwidth and data from military radar and electronic warfare systems is continuing to put pressure on embedded signal processing designers to deliver innovation at the board and chip level. In this podcast, David Gamba, Aerospace and Defense Core Vertical Markets Director at Xilinx, discusses how FPGAs enable this innovation especially from an RF system-on-chip (SoC) perspective.

Click **here** to listen to the podcast.

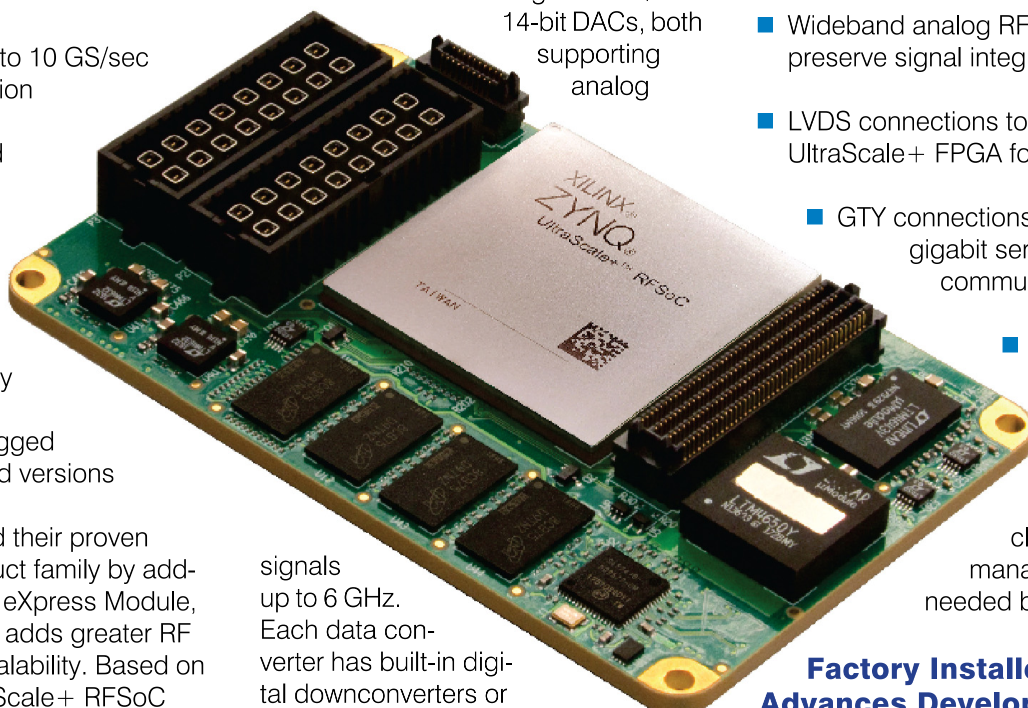
Pentek Announces Immediate Availability of Higher Bandwidth Gen 3 RFSoC Solutions

- Pentek Quartz® Architecture with Xilinx® Zynq® UltraScale+ ™ RFSoC Gen 3
- Digitizes RF Input Signals up to 6 GHz at 5 GS/sec with 14-bit resolution
- DAC sample rate to 10 GS/sec with 14-bit resolution
- Built-in, expanded decimation and interpolation
- Supported by Pentek's Navigator® BSP, FDK and IP Library
- Air-cooled and rugged conduction-cooled versions

Pentek has extended their proven Quartz RFSoC product family by adding a new QuartzXM eXpress Module, **Model 6003**, which adds greater RF performance and scalability. Based on the Xilinx Zynq UltraScale+ RFSoC Gen 3, Model 6003 provides full sub-6 GHz direct-RF I/O support and greater flexibility with more decimation and interpolation options. The Model 6003 is ideal for 5G and LTE wireless, SIGINT, EW, communications, and radar applications in SWaP-critical environments.

"Immediately releasing products utilizing Xilinx Zynq UltraScale+ RFSoC Gen 3 demonstrates our commitment to offering our customers the latest technology for their applications," said Bob Sgandurra, Pentek's director of Product Management. **"The modularity of our Quartz product line enables us to quickly provide solutions in any form factor needed – whether it's in the lab or in a deployed application."**

QUARTZ



These new Quartz products support direct RF sampling using 5 GS/sec 14-bit ADCs and eight 10 GS/sec 14-bit DACs, both supporting analog signals up to 6 GHz. Each data converter has built-in digital downconverters or upconverters with programmable decimation and interpolation up to 40x and independent tuning for increased RF flexibility and frequency planning.

The Quartz Architecture Difference

The Pentek Quartz architecture positions the RFSoC as the cornerstone of the design. All control and data paths are accessible by the RFSoC's programmable logic and processing system. The Xilinx Zynq UltraScale+ RFSoC Gen 3 integrates eight RF-class ADCs and DACs into the Zynq FPGA fabric along with quad ARM Cortex-A53 and dual ARM Cortex-R5 processors, creating a multichannel data conversion and processing solution on a single chip.

Complementing the RFSoC's on-chip resources, the QuartzXM Model 6003 adds:

- Wideband analog RF connectors to preserve signal integrity
- LVDS connections to the Zynq UltraScale+ FPGA for custom I/O
- GTY connections for 28 Gbaud gigabit serial communication
- 16 GBytes of DDR4 SDRAM
- All power supplies and clocking management needed by the RFSoC

Factory Installed IP Advances Development

The QuartzXM Model 6003 is preloaded with a suite of Pentek IP modules to provide data capture and processing solutions for many common applications. Modules include DMA engines, DDR4 memory controller, test signal and metadata generators, data packing and flow control. The board comes pre-installed with IP for triggered waveform and radar chirp generation, triggered radar range gate engine, wideband real-time transient capture, flexible multi-mode data acquisition, and extended decimation.

The Quartz Family Versatility

These enhancements will be available across the entire Quartz family of Zynq UltraScale+ RFSoC eight-channel ➤

A/D & D/A converter products. The first products to be available are:

- **Model 6003** QuartzXM Module
- **Model 5953** 3U OpenVPX Board
- **Model 6353** Small Form Factor Rugged Enclosure
- **Model 7053** PCIe Board
- **Model 5553** SOSA-Aligned 3U OpenVPX Board

These Quartz products can be deployed as out-of-the-box solutions with built-in functions requiring no FPGA development, and are available for air-cooled, conduction-cooled, and rugged operating environments.

Carrier Design Kit

The Design Kit supports customers interested in building their own carrier for the QuartzXM Model 6003. The kit encapsulates all of Pentek's electrical and mechanical design knowledge to accelerate application-specific carrier design. The kit includes a review of the customer's design with Pentek's engineering staff; pin definitions and electrical specifications of all signals on the module; 3D models of the module; thermal profiles of the module and components; carrier reference design schematics; PCB stack-up recommendations; PCB design guidelines and routing rules; operating system and bootstrap guidelines.

Streamlined IP Development

Pentek's Navigator Design Suite includes: Navigator FDK (FPGA Design Kit) for custom IP and Navigator BSP (Board Support Package) for creating host software applications.

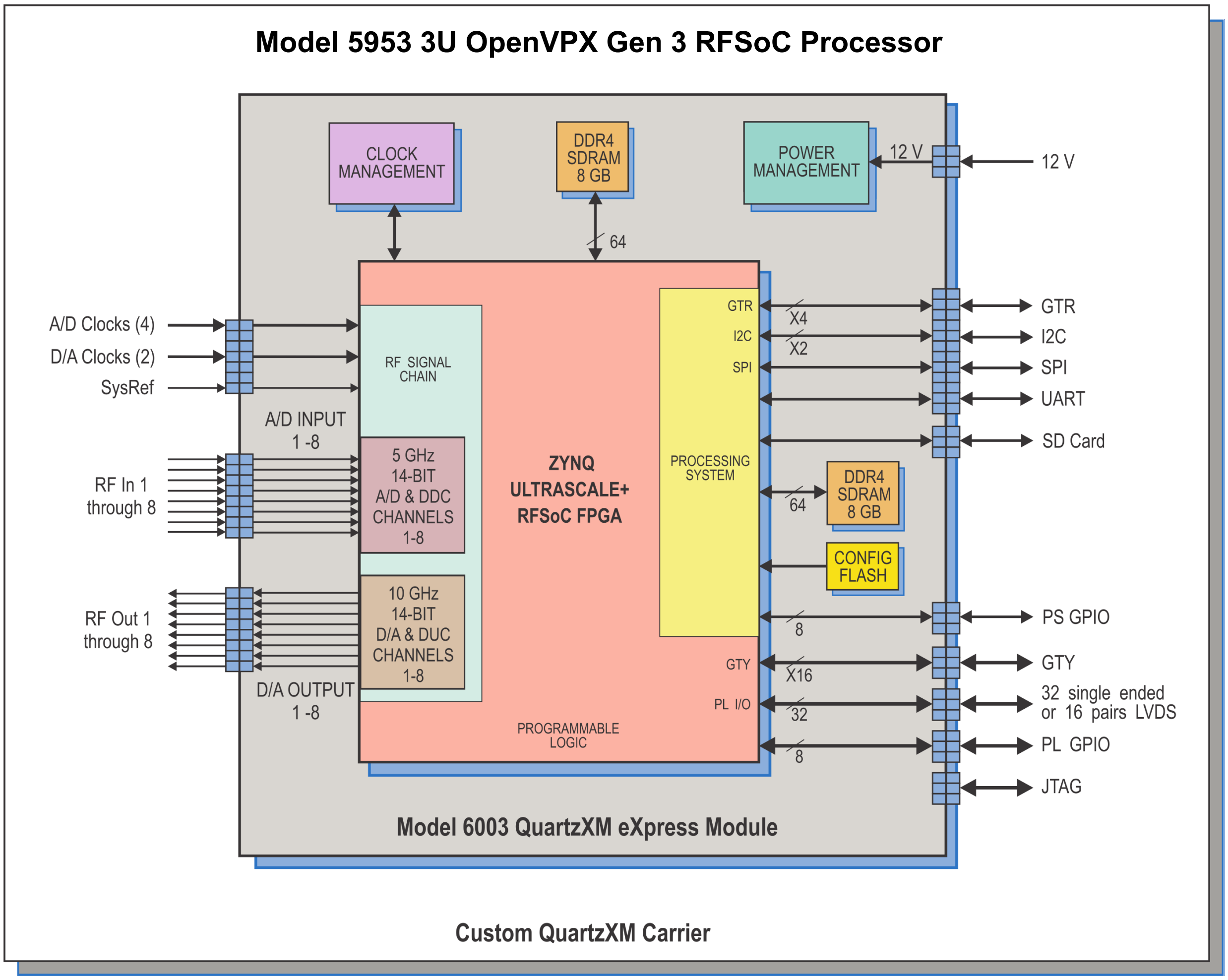
The Navigator FDK includes the board's entire FPGA design as a block diagram that can be graphically edited in Xilinx's Vivado tool suite, with full source code and documentation. Developers can integrate their IP along with the factory-installed functions or use the Navigator kit to replace the IP with their own. The Navigator FDK Library is fully AXI-4 compliant, providing a well-defined interface for developing custom IP or integrating IP from other sources.

The Navigator BSP supports Xilinx's PetaLinux on the ARM processors. Users can work efficiently using high-level API functions, or gain full access to the underlying libraries including source code. Pentek provides numerous examples to assist in the development of new applications.

Whether the QuartzXM is deployed on a Pentek carrier or a custom carrier, developers will find the included IP cores and examples an ideal foundation for building custom applications.

The QuartzXM Model 6003 and Quartz Model 5953 are immediately available. Quartz Models 6353 and 7053 will be available in Q1 2021. The Quartz Model 5553 will be available in Q2 2021.

To learn more about these products, please contact our sales department at sales@pentek.com, 201-818-5900 or contact your local representative. ☐



Quartz RFSoC Rugged Small Form Factor Enclosure Ideal for Harsh Environments

- Pentek Quartz® Architecture with Xilinx® Zynq® UltraScale+ ™ RFSoC FPGA
- Eight wideband A/D and D/A converters
- Optional dual optical MPO 100 GbE interfaces stream data at 25 GB/sec
- Navigator® Design Suite for streamlined software and IP development

Pentek has announced an addition to the Quartz RFSoC Architecture family: **Model 6350**, an eight-channel A/D and D/A converter system in a rugged small form factor (SFF) enclosure. Based on the Xilinx Zynq UltraScale+ RFSoC, the Model 6350 is very suitable for SIGINT and COMINT, military communications, EW countermeasures, radar transceiver, test and measurement, SATCOM, LiDAR, 5G and LTE wireless applications.

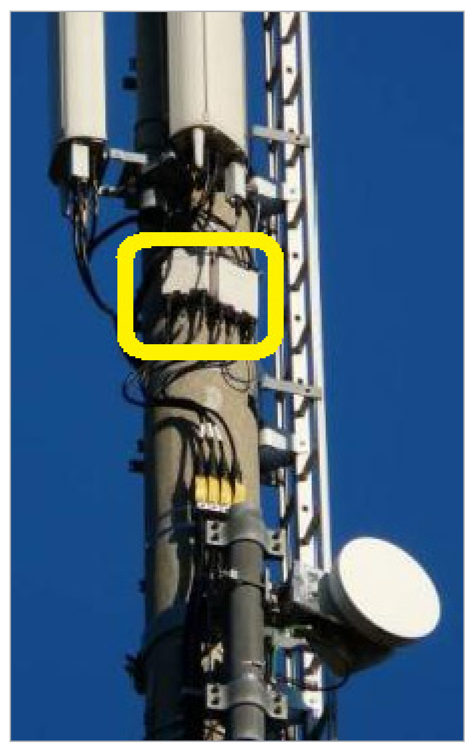
"Because Quartz RFSoC products are extremely popular with our customers, we were getting requests to use these Quartz products in harsher environments. The Model 6350 is a self-contained system in a SFF enclosure that allows for deployment in rugged installations." said Bob Sgandurra, director of Product Management of Pentek. He added, **"Our QuartzXM eXpress module, the heart of the Quartz family, enables us to quickly adapt to new form factors for our customers. This Model 6350 system provides a ruggedized, weatherized, space-constraint solution to many applications and extends this functionality for pods, UAVs, antenna masts, and other remote or space-constrained installations."**

Designed for Harsh Environments

Optimized for SWaP (size, weight and power), the Model 6350 measures 3.53" H, 5.65" W, 9.57" D and weighs in at just under 8 pounds. Intended for use in rugged environments, the Model 6350 is designed to the IP67 specification (Ingress Protection Code, IEC standard 60529) for dust and water immersion. The internal 'I-beam' construction creates a chassis that is both extremely rugged and efficient for moving heat out of the box, making it ideal for deployment in the harshest environments and well matched to conduction-cooled installations. The Model 6350 can also be used with an optional fan plate for desktop development.

The Quartz Architecture Difference

The Pentek Quartz architecture embodies a streamlined approach to FPGA products, simplifying the design for reduced power and cost, while still providing some of the highest performance FPGA resources available today. Supported by Pentek's Navigator Design Suite tools, Quartz products offer users an efficient path for developing and deploying software and FPGA IP for data and signal processing. The Xilinx Zynq UltraScale+ RFSoC Processor integrates eight RF-class A/D and D/A converters into the Zynq FPGA fabric along with quad ARM Cortex-A53 and dual ARM Cortex-R5 processors, creating a multichannel data conversion and processing solution on a single chip. ➤



Antenna Mast Deployment Example

Factory Installed IP Advances Development

The Model 6350 is pre-loaded with a suite of Pentek IP modules to provide data capture, timing, interface, and processing solutions for many common applications. Modules include DMA engines, DDR4 memory controllers, test signal and metadata generators, data packing, and flow control. The board comes pre-installed with IP for triggered radar chirp generator, triggered radar range gate engine, wideband real-time transient capture, flexible multi-mode data acquisition, and extended decimation. The Model 6350 can be used out-of-the-box with these built-in functions, requiring no FPGA development.

Data Conversion

The front end accepts analog IF or RF inputs on eight external SMA connectors with transformer-coupling to eight 4 GSPS 12-bit A/D converters, delivering either real or complex DDC samples. With additional IP-based decimation filters, the overall DDC decimation is programmable from 2 to 128. The eight D/A converters accept baseband real or complex data streams from the FPGA's programmable logic. Each 6.4 GSPS 14-bit D/A includes a digital upconverter with independent tuning and interpolations of 1x, 2x, 4x and 8x. Each D/A output is transformer-coupled to an SMA connector. The Model 6350's simplified connector scheme provides full access to control, data, and power using environmentally rugged connectors.

The Model 6350 supports eight 25 Gb/sec full duplex optical lanes to a miniature rugged circular connector. With the built-in 100 GigE UDP interface or installation of a user-provided serial protocol, this optical interface enables a high-speed gigabit data streaming path between the Model 6350 and data storage or processing subsystems.

Navigator Design Suite for Streamlined IP Development

Pentek's Navigator Design Suite includes: Navigator FDK (FPGA Design Kit) for custom IP and Navigator BSP (Board Support Package) for creating host software applications.

The Navigator FDK includes the board's entire FPGA design as a block diagram that can be graphically edited in Xilinx's Vivado tool suite, with full source code and documentation. Developers can integrate their IP along with the factory-installed functions or use the Navigator kit to replace the IP with their own. The Navigator FDK Library is fully AXI-4 compliant, providing a well-defined interface for developing custom IP or integrating IP from other sources.

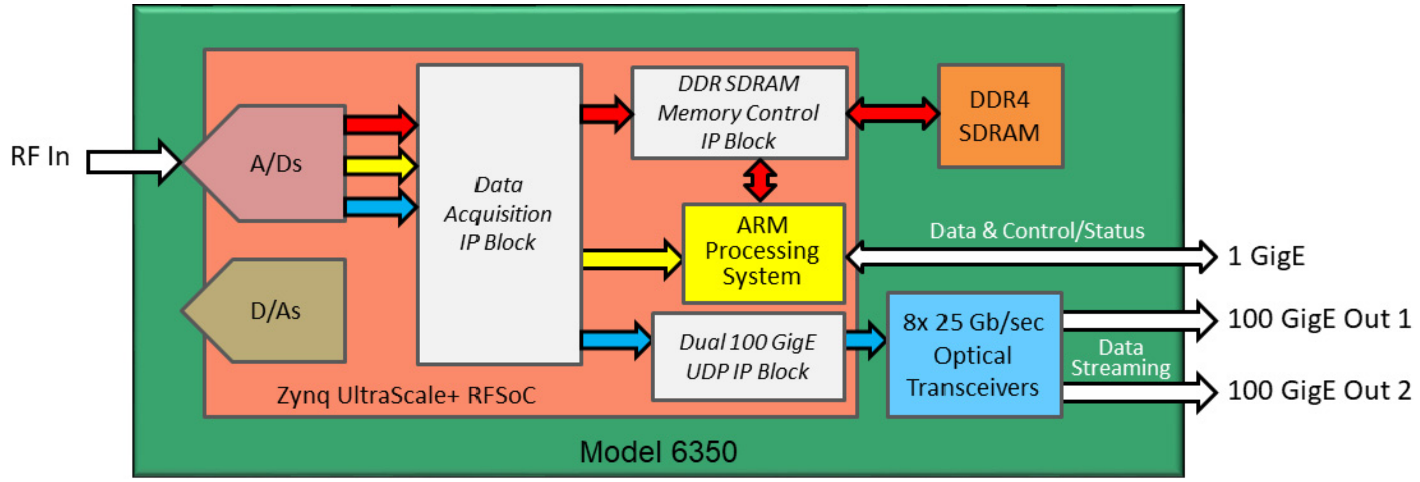
The Navigator BSP supports Xilinx's PetaLinux on the ARM processors. Users can work efficiently using high-level API functions, or gain full access to the underlying libraries including source code. Pentek provides numerous examples to assist in the development of new applications.

Example Applications

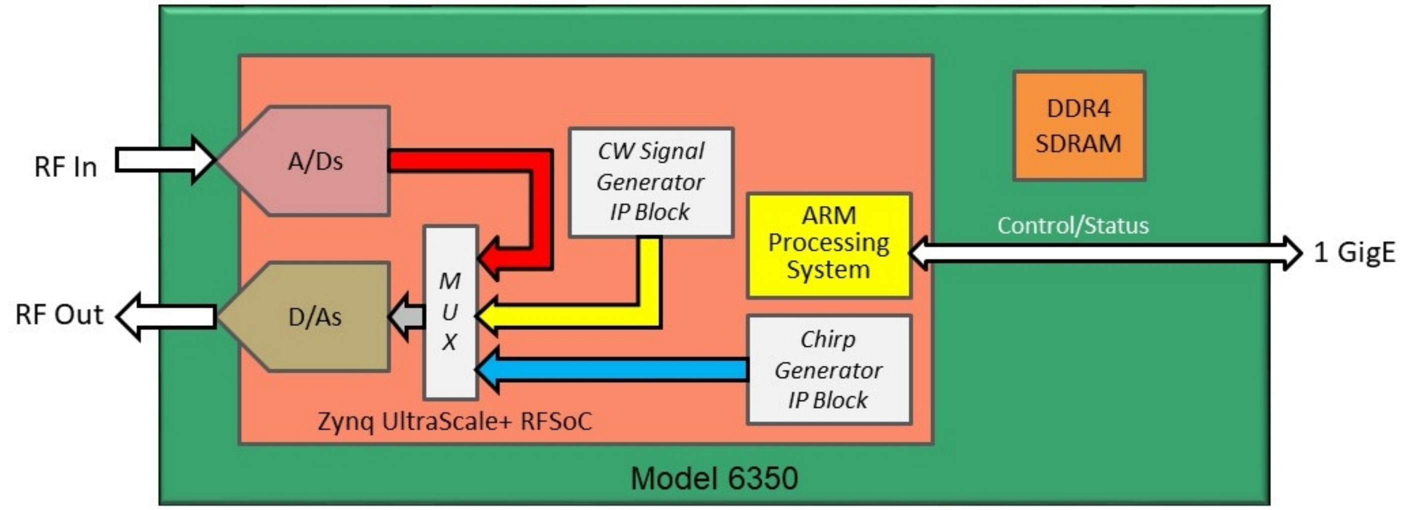
Two example applications using the Pentek Model 6350 are described below. For each example, the board's included IP is all that is needed to demonstrate the application and may satisfy the full set of requirements for any particular application. These applications can also be the starting point for adding additional IP from the Pentek Navigator IP library or for adding custom IP.

Example 1: High Bandwidth Data Streaming

The RFSoC's eight 4 GSPS A/Ds are capable of producing an aggregate data rate of 64 GB/sec when all channels are enabled. While capturing this much raw data is not feasible, the A/Ds' built-in digital downconverters can reduce this data throughput in many applications to a rate reasonable for the data streaming and storage ➤



Example Application 1



Example Application 2

components downstream in the system.

In some applications, capturing the raw, full bandwidth data is crucial. The 6350's dual 100 GigE UDP engine provides a high bandwidth path for moving data off of the board (shown with blue arrows). Along with the built-in data acquisition IP, the 6350 can stream two full bandwidth A/D data streams over optical cable to a downstream storage or processing subsystem.

The 6350's built-in IP functions also provide paths for capturing data in the DDR4 SDRAM memory for retrieval by the ARM processing system or the FPGA programmable logic (shown with red arrows) and for sending data over the ARM's 1 GigE interface (shown in yellow arrows).

Example 2: Analog Loopback and Waveform Generator

The 6350's IP supports multiple D/A signal source options. A simple loop-back path allows samples received by the A/Ds to be output through the D/As (shown with a red arrow) . A CW signal generator produces a sine output with programmable frequency (shown with a yellow arrow). A chirp generator, ideal for radar applications, outputs sweep signals with programmable frequency, ramp, phase offset, gain offset and length (shown with a blue arrow). The generators also include flexible trigger options with both internal and external triggering.

For more information ...

To learn more about Model 6350, please contact our sales department at sales@pentek.com, 201-818-5900 or contact your local representative. □

Military & Aerospace Electronics and Intelligent Aerospace have announced their **2020 Technology Innovators Awards** to recognize companies offering substantial military, aerospace, and avionics design solutions and…

Pentek's **Model 6001 8-Channel A/D & D/A Zynq UltraScale+ RFSoC Processor QuartzXM module** won **Gold**!

Model 6001 is the heart of Pentek's Quartz products. To learn more about Model 6001, **click here**.

New Video about Quartz!

Click below to learn more about Pentek's Quartz family of Xilinx Zynq UltraScale+ RFSoC FPGA Products.

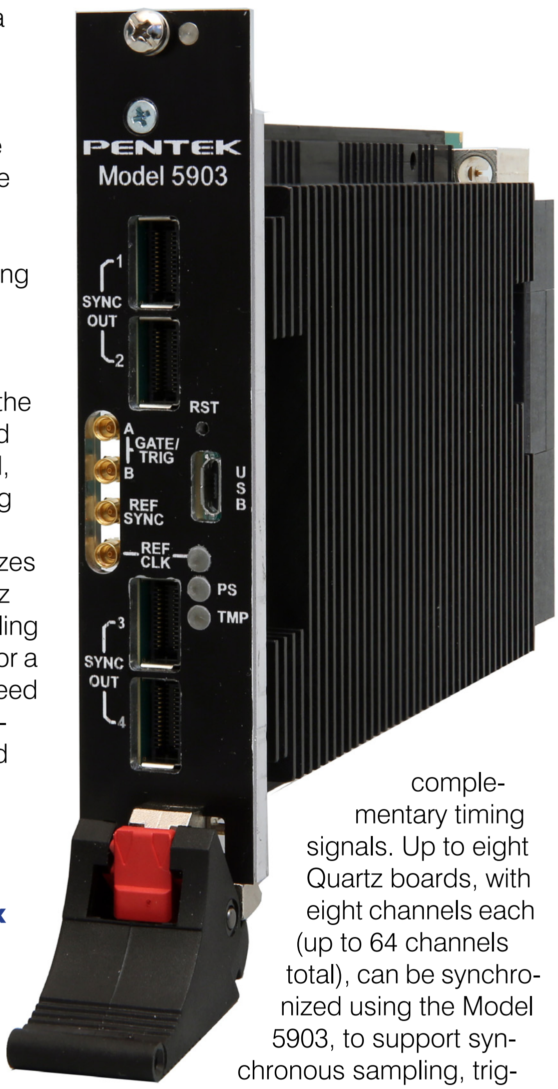
High-Speed Synchronizer and Distribution Board for Quartz RFSoC Products

- Synchronizes up to 64 channels across eight Quartz® boards
- Synchronizes sampling and data acquisition for multichannel systems
- Provides single sample accurate synchronization between multiple channels and multiple boards
- Synchronizes gating and triggering functions

Pentek has added a board to the Quartz RFSoC Architecture family: the **Model 5903**, a 3U VPX high-speed synchronizer and distribution board, optimized for Pentek products using the Xilinx® Zynq® UltraScale+ ™ RFSoC. The Model 5903 synchronizes up to eight 8-channel Pentek Quartz family boards within a system, enabling synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, radar, beamforming, 5G, electronic warfare, and software radio applications.

"The Model 5903 solves a challenging problem for designers developing complex systems," said Bob Sgandurra, director of Product Management of Pentek. He added, **"The Xilinx RFSoC offers extraordinary capabilities, but it's complicated to precisely synchronize multichannel configurations. Our engineers have solved this challenge so that customers with high-channel-count phase-coherent applications can immediately start development without having to work out synchronization strategies."**

An on-board programmable clock generator creates the sample clock and



complementary timing signals. Up to eight Quartz boards, with eight channels each (up to 64 channels total), can be synchronized using the Model 5903, to support synchronous sampling, triggering and gating functions across all boards.

The Model 5903 provides four front panel MMCX connectors to accept input signals from external sources: one for reference clock, one for sync and two for gate/trigger signals. The internal programmable clock generator can create sample clock frequencies from 1 to >5 GHz. The sample clock can be locked to the internal 100 MHz frequency reference or locked to an external reference input connector. Similarly, sync and gate/trigger signals can be generated on-board via software or received from external sources through the sync and gate/trigger input connectors.

All board modes and operations are controlled by an on-board processor. Commands to this processor are sent via USB either through a front panel port or through the Rear Transition Module (RTM). The Pentek Navigator® BSP provided with Quartz boards includes configuration utilities for the Model 5903.

The Model 5903 delivers a multi-signal sync bus to each board to be synchronized, containing sample clocks, reference clocks, and gate/trigger and sync signals. Four sync buses are provided on the Model 5903's front panel and four are provided to the VPX backplane and optionally to an RTM. Connections between boards are facilitated across the VPX backplane and through precision matched multi-signal sync cables that come with the Model 5903.

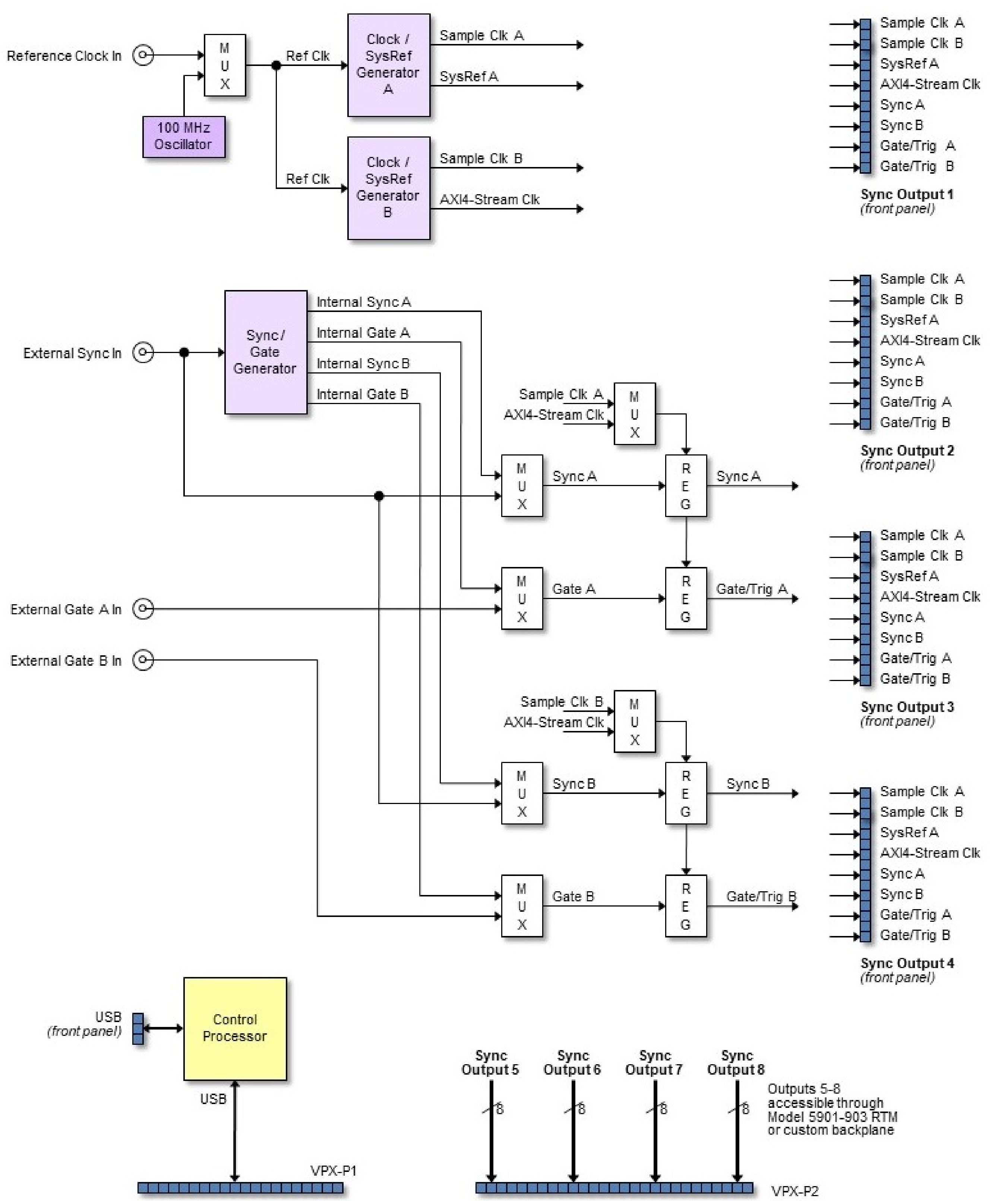
The Model 5903 is ideal for use with Pentek's 8-Channel A/D and D/A boards based on the Zynq UltraScale+ RFSoC processor: Models 5950 & 5953 3U VPX boards and the Model 7050 & 7053 PCIe boards.

The Model 5903 block diagram and two sample system configurations are shown on the next two pages.

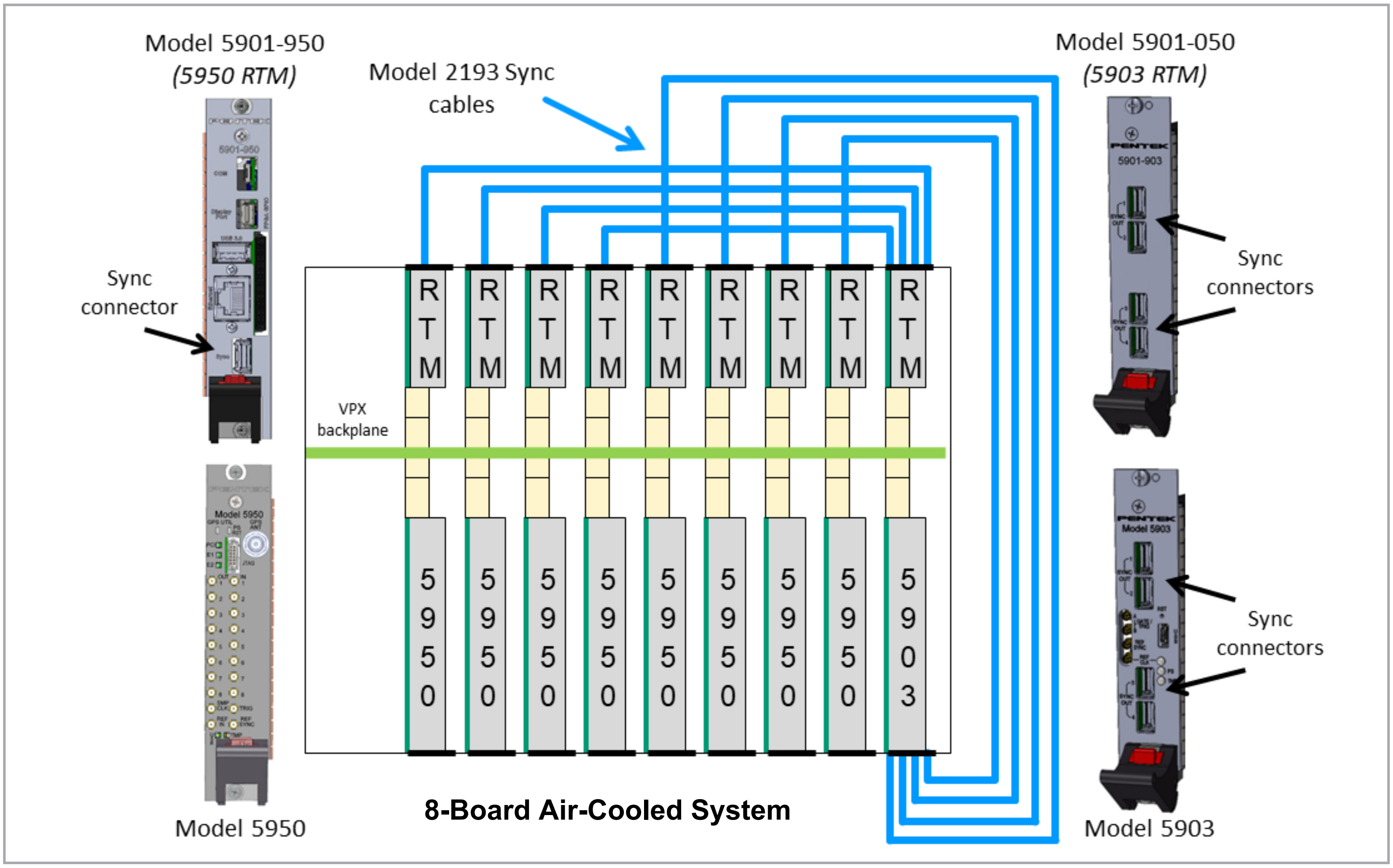
For more information about Model 5903, click here.

You also can email us at sales@pentek.com, contact your local representative, or contact Pentek directly [+1 (201) 818-5900]. ☐

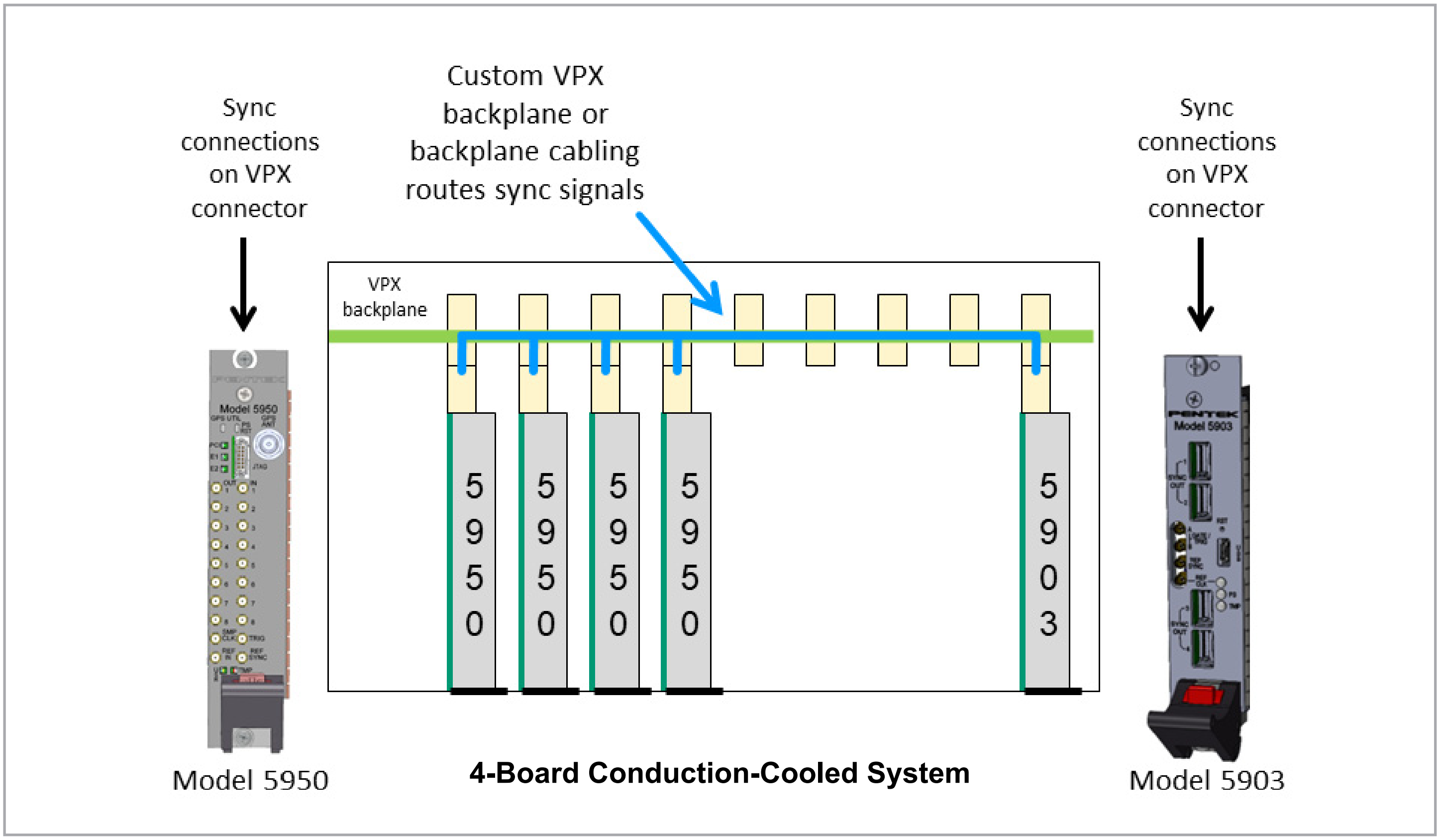
Model 5903 Block Diagram



System Configurations



8-Board Air-Cooled System



4-Board Conduction-Cooled System

Pentek's New 6 GHz Ultra-Wideband Talon RF/IF Recorder Extends Recording Bandwidths

- Sample rates up to 6 GHz
- Real-time sustained recording rates up to 6 GB/sec
- Analog signal bandwidths up to 2.4 GHz for recording and 1.28 GHz for playback
- Front-panel removable NVMe storage up to 122 TB
- SystemFlow® software GUI with Signal Viewer analysis tool

Pentek has announced a new addition to the Talon® Series of recorders, the **Model RTR 2742** 4U 19-inch rackmount recorder. The Talon RTR 2742 is a turn-key record and playback system for ultra-wideband analog RF/IF signals. Using two 12-bit, 6.4 GHz A/D converters, this system can achieve sustained recording of 2.4 GHz bandwidth signals at rates up to 6 GBytes per second. It can be configured as a one- or two-channel system and can record real samples or complex I+Q digitally down-converted samples.

Complemented by a 16-bit, 6.4 GHz D/A converter, the RTR 2742 is capable of playing back analog signal bandwidths up to 1.28 GHz. Built-in digital down- and up-converters provide flexible bandwidth and tuning frequency selection for both record and playback.

"Many communications and radar applications operate across ultra-wideband frequencies. Now we can satisfy the many customers who need to digitize and record these signals with bandwidths as high as 2.4 GHz," noted Rodger Hosking, vice-president, Pentek. He added, **"With the Talon RTR 2742, engineers can capture the whole spectrum in a single wideband channel, eliminating the need to break up the signal into multiple smaller bands occupying adjacent slices of the spectrum."**

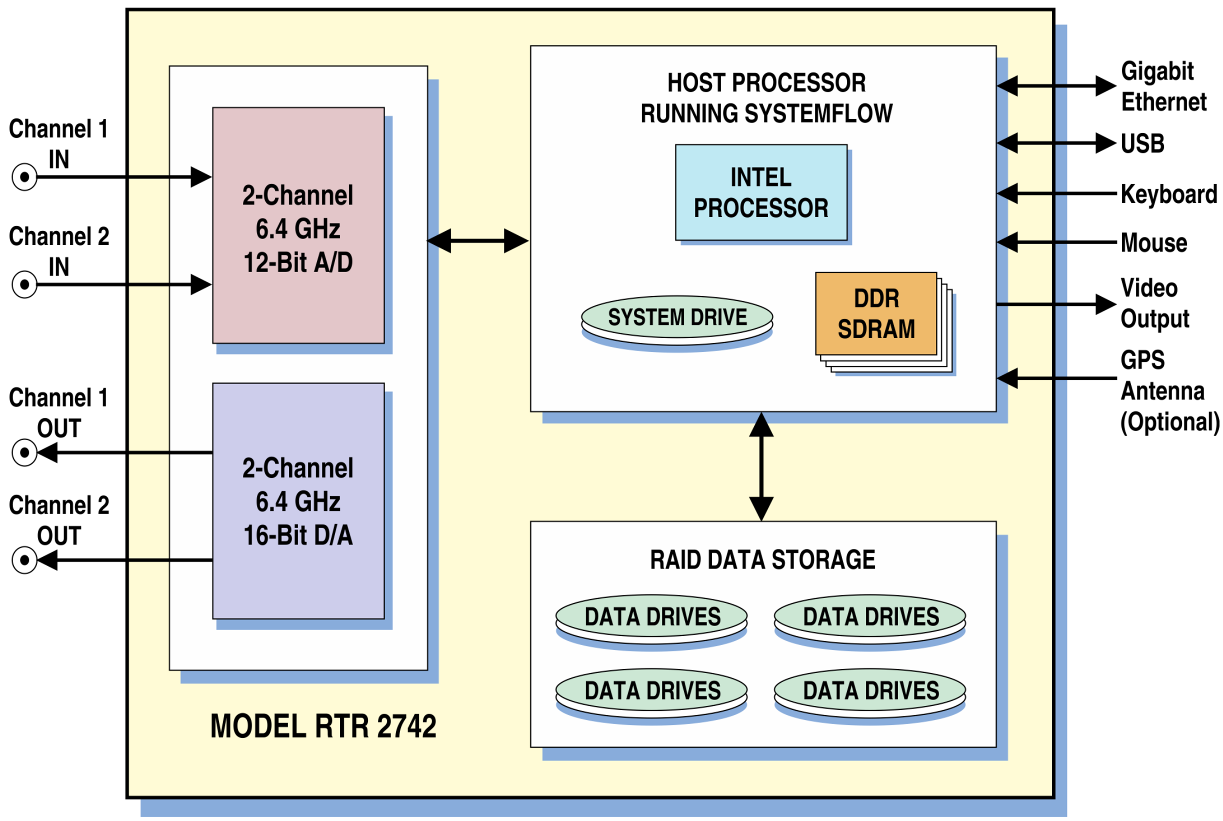
The industrial grade 4U 19-inch rackmount chassis of the RTR 2742, with hot-swappable data drives, front-panel USB ports and I/O connectors on the rear panel, is optimized for cooling and ruggedized to operate in challenging environments.

The RTR 2742 includes a 12-bit 6.4 GHz A/D that can be clocked at rates from 1.6 to 6 GHz in single-channel mode. Data can be truncated and packed as 8-bit samples, to support continuous recording up to the maximum sample rate. The D/A is capable of reproducing signals with up to 1.28 GHz of instantaneous bandwidth and includes a wide range of interpolations. The RTR 2742 provides up to 122 TB of front panel removable solid-state storage for hours of real-time, high-bandwidth signal recording.

Ease of Operation

All Talon recorders are built on a Microsoft Windows platform and include Pentek's SystemFlow software, featuring a GUI (graphical user interface), the Signal Viewer and API (Application Programming Interface). The GUI provides intuitive controls for out-of-the-box turn-key operation using point-and-click configuration management.

Configurations are easily stored and recalled for single-click setup. The Signal Viewer provides a virtual oscilloscope and spectrum analyzer to monitor signals before, during and after data collection. The C-callable API allows users to integrate the recorder control into larger application systems. Enhancements to the GUI allow more efficient configuration of the recording channels.



The data format used for storage follows the NTFS standard, allowing users to remove drives from the instrument and read the data using standard Windows-based systems, eliminating the need for file format conversion.

Free Demo

Pentek provides a Talon Recording System Simulator for evaluation of the SystemFlow software package. Click here to download this free trial package.

Talon Family Summary

- **RTV Value Series:** Low-cost rackmount systems for laboratory environments
- **RTS Commercial Series:** Rackmount systems for laboratory environments
- **RTR Portable Series:** Rugged portable systems for field use
- **RTR Rackmount Series:** Rugged rackmount systems for field use
- **RTX Extreme Series:** Rugged systems for extreme environments

For more information about Talon Model RTR 2742, click here. You also can email us at sales@pentek.com, contact your local representative, or contact Pentek directly [+1 (201) 818-5900]. ☐