The Pentek Pipeline

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A quarterly publication for engineering system design and applications.

In This Issue

- **Feature:** Two years ago, we published an artcle about VITA 49 that described how the VITA 49 Radio Transport (VRT) protocol addressed the challenges inherent in traditional software radio architecture. This updated article describes how VRT has evolved and improved via VITA 49.2.

"Before VRT, systems relied on complicated local interfaces between the receiver and the processor to ensure coherency for a given task. VRT provides an elegant solution by encapsulating parameter and timing information along with the data."

Rodger Hosking, Pentek Vice President and Co-founder

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VITA 49: The Future of Software Radio, Part 2

by Rodger Hosking, Pentek, Inc.

The use of software radio technology has spread to almost every commercial, consumer, government, industrial, and military platform across the entire radio frequency spectrum during the technology's 25-year lifespan. Innovations in data converter technology, DSP devices, system interconnects, processors, software, design tools, and packaging techniques have improved performance levels and reduced the size, weight, and power consumption of software radio systems. However, the rapid surge in software radio applications spawned ad hoc, proprietary interfaces between the elements in these systems.

More than ten years ago, government and military customers realized this complexity was undermining software radio's reliability and maintainability as well as hindering feature upgrades and technology refresh cycles. They also wanted to improve compatibility between vendors and reuse software radio hardware platforms for different types of signals and new applications in the future. So those interested in addressing these issues started work on VITA 49.0, which became known as VRT, for VITA Radio Transport.

This article describes how VRT has evolved and improved in the past several years via VITA 49.2. This article is an update to a VITA 49 article we published two years ago. To read the original version, click here.

VRT Evolves and Improves via VITA 49.2

Approved as an ANSI standard in 2007, VITA 49.0 represented the first official standard for VRT, but it only defined receiver functions using the VRT IF Data and Context packets. After demonstrating its usefulness by early adopters, system designers wanted to extend its scope to encompass even more elements of software radios. The original VITA 49.0 standard omits support for transmitters, control and status functions, and any signals other than digital IF. To address these shortcomings, VITA 49.2 was initiated with new packet classes represented in **Figure 2** on page 2.

Signal Data Packets

The original IF Data Packet is replaced with the Signal Data Packet, which not only supports digitized IF signals, but also ➢

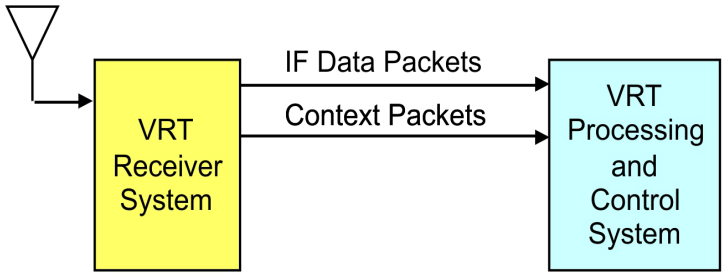


Figure 1. VITA 49.0 System Overview with IF Data Packets and Context Packets

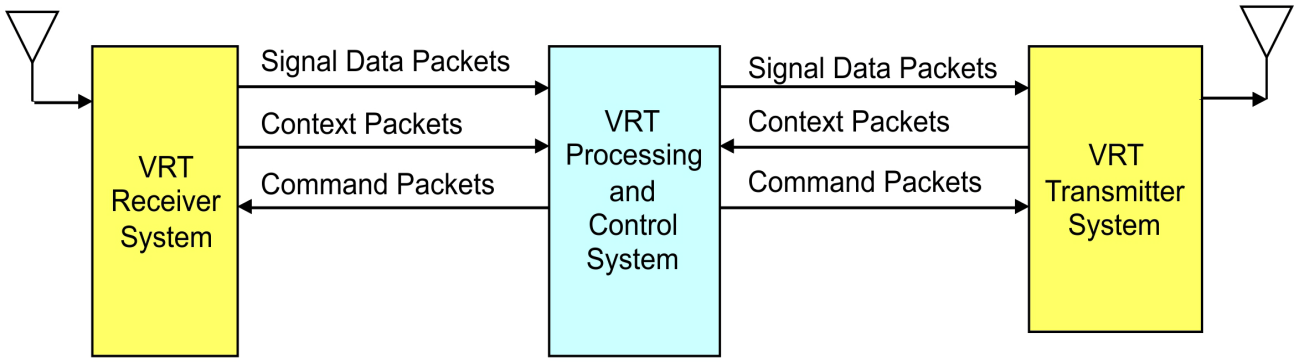


Figure 2. VITA 49.2 Under Development Adds Control, Acknowledgment, Capabilities, and Transmitter Packets

baseband signals, broadband RF signals, and even spectral data. Signal Data Packets are backwards compatible with IF Data Packets, with new identifier bits to specify the data type.

To support bi-directional radio signals, Signal Data Packets can now be used for transmit data, supporting baseband, IF, and RF signals. Here, the time stamp dictates the transmit time, which is especially useful for generating precisely-timed radar pulses. Multi-static radar systems use one antenna for transmitting pulses and other remotely located antennas for capturing the reflected pulses. Through GPS synchronization, VRT can be used to coordinate transmit and receive signals at each site.

Spectral survey systems are in widespread use for detecting and recording signals of interest. Under VITA 49.2, Signal Data packets can carry digitized spectral information from scanning receivers, and deliver packets to analysts anywhere in the world. These packets maintain full context information regarding location, circumstances and conditions, as well as a precise time stamp.

Enhanced Context Packets

The original Context Packet is also significantly enhanced in VITA 49.2. Many more types of metadata are supported for new details and richer information about the signal data. Context Packets now allow a VRT resource to respond to the system with a complete set of its operational specifications including minimum and maximum limits of each programmable parameter. This may include frequency tuning range, bandwidth settings, range of programmable gain, antenna azimuth angle limits, and range of transmit power levels.

Context Packets now also provide additional characteristics such as:

- the settling time when switching tuning frequency, bandwidth, or gain
- the angle slew rate for a movable dish antenna
- frequency accuracy and stability
- time stamp and ephemeris accuracy
- operating temperature range
- tolerance limits for shock and vibration
- the effects of temperature drift and aging. ➢

In theory, a VITA 49.2 System Processor can connect to a new, unknown software radio resource and automatically discover everything it can do, how to control and monitor its operation, and how to successfully exchange receive and transmit signals. In practice, Context Packets will be most useful when developing new applications on existing platforms, and in reacting responsibly to new threats or circumstances during deployed operations.

Gaining Control with Command Packets

Another deficiency of VITA 49.0 was its lack of control of software radio resources. VITA 49.2 adds a new packet class called Command Packets, which allow the VRT System Processor to deliver operating parameters to each element using the same standardized fields and formats as the Context Packets. This provides a consistent control interface across a wide class of hardware, ranging from antenna positioning systems to transmit power amplifiers.

Command packets not only provide control, but also support status and acknowledgement functions so that the VRT processor can check the operational status of the receivers and transmitters to verify successful execution of the control commands.

This comprehensive and complimentary control/status protocol of VRT provides an essential function for cognitive radio, adaptive spectral management, electronic counter measures, and other critical applications.

Extension Packets

Because of the diverse requirements across EW, SIGINT, radar, and communications systems for both military and commercial markets, VITA 49.2 adds Extension Packets, which are intended to convey application-specific information that is otherwise not supported in any existing Context Packet fields.

VRT Benefits Key Applications

Software radio SIGINT and COMINT systems attempting to locate, identify, and monitor a wide range of unknown signals can extract many useful facts from the VRT Information Stream. These can include the azimuth and elevation of a directional antenna, the reference power level of the RF signal, the bandwidth and tuning frequencies of the RF tuner and DDC, the sample rate of the ADC, the frequency accuracy of the RF tuner and sample clock, a signal ID tag, and the time stamp.

Particular emphasis is devoted to time stamp accuracy. VRT time stamps allow beamforming applications to compare absolute time and phase differences between signals received from multiple antennas to calculate distance, location, speed, and heading of a transmitter. Likewise, a multi-element diversity receiver can exploit VRT time stamps to create delays and phase shifts in each antenna signal path to maximize receptivity in a particular direction.

Absolute time can be derived from GPS receivers, so that software radio receivers separated by great distances can be synchronized to capture signals at the same time. This can be very useful for tracking signals from satellites or even from sources in deep space.

Radar systems must capture reflected pulses during precise intervals of time relative to the outgoing radar pulse, usually defined as a range gate. When the received data is captured, VRT delivers a time stamp to the radar processing engine, showing the exact arrival time of the return signal.

Before VRT, systems relied on complicated local interfaces between the receiver and the processor to ensure coherency for a given task. VRT provides an elegant solution by encapsulating parameter and timing information along with the data. A major benefit here is that the VRT Information Stream can be delivered to any number of remote processing facilities, while fully preserving the critical metadata and time stamp.

Like any successful standard, VITA 49 continues to evolve as new technology emerges and through feedback from real-world deployment. With so many clear benefits and relatively little extra complexity, VRT is expected to mark the trail for new and future software radio systems. ❐

Pentek is Now a Member of the Association of Old Crows

With over 13,000 members internationally, the **Association of Old Crows** is an organization for individuals who have common interests in Electronic Warfare (EW), Electromagnetic Spectrum Management Operations, Cyber Electromagnetic Activities (CEMA), Information Operations (IO), and other information related capabilities. The Association of Old Crows provides a means of connecting members and organizations nationally and internationally across government, defense, industry, and academia to promote the exchange of ideas and information, and provides a platform to recognize advances and contributions in these fields.

ASSOCIATION OF OLD CROWS

Pentek's Jade™ Model 71132

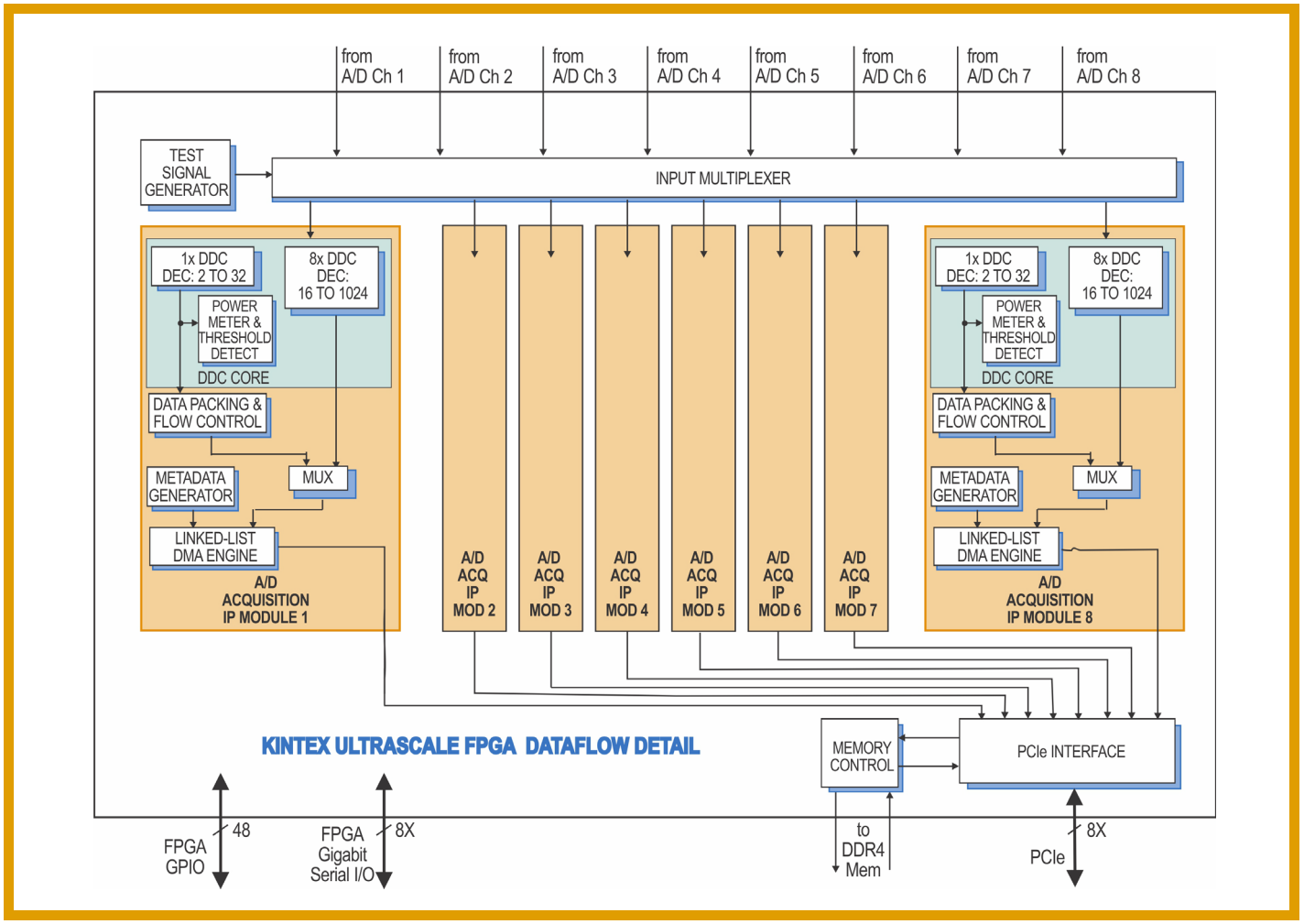
8-Channel 250 MHz A/D XMC Module with 72 DDCs for Defense and Radar Phased-Array Applications

Pentek has announced a new member of the Jade™ family of high-performance data converter XMC modules based on the Xilinx Kintex Ultrascale FPGA. The **Jade Model 71132** features eight 250 MHz 16-bit A/Ds with eight wideband digital down converters (DDCs) and 64 multiband DDCs, all fully programmable.

Model 71132 increases the number of DDCs by a factor of nine over the previous model, giving this the best price per channel ratio in the product family. Applications monitoring a broad spectrum with a need to quickly analyze specific portions of the identified spectrum can greatly benefit from the capabilities of the 71132.

Performance IP Cores

The 71132 factory-installed functions include eight A/D acquisition IP modules, each containing nine DDCs. In each module, the wideband DDC supports decimations from 2 to 32 for capturing signal bandwidths up to 100 MHz. The eight narrowband DDCs allow decimations up ➢



to 1024 for signal bandwidths down to 200 kHz. These two types of DDCs operating in parallel are ideal for applications that need to monitor a wide spectrum but quickly tune to identified frequency bands of interest for further analysis.

"We continue to expand our factory-installed FPGA functions to boost DDC channel density and add new operational modes for our customers, right out of the box." said Bob Sgandurra, director of Product Development of Pentek. ***"The Navigator FPGA Design Kit (FDK) includes a wealth of Pentek IP library modules so customers can easily add custom IP to support specific needs. The Model 71132 is a very cost-effective solution for applications that need many DDCs to capture both wide and narrow frequency bands."***

The Jade Architecture

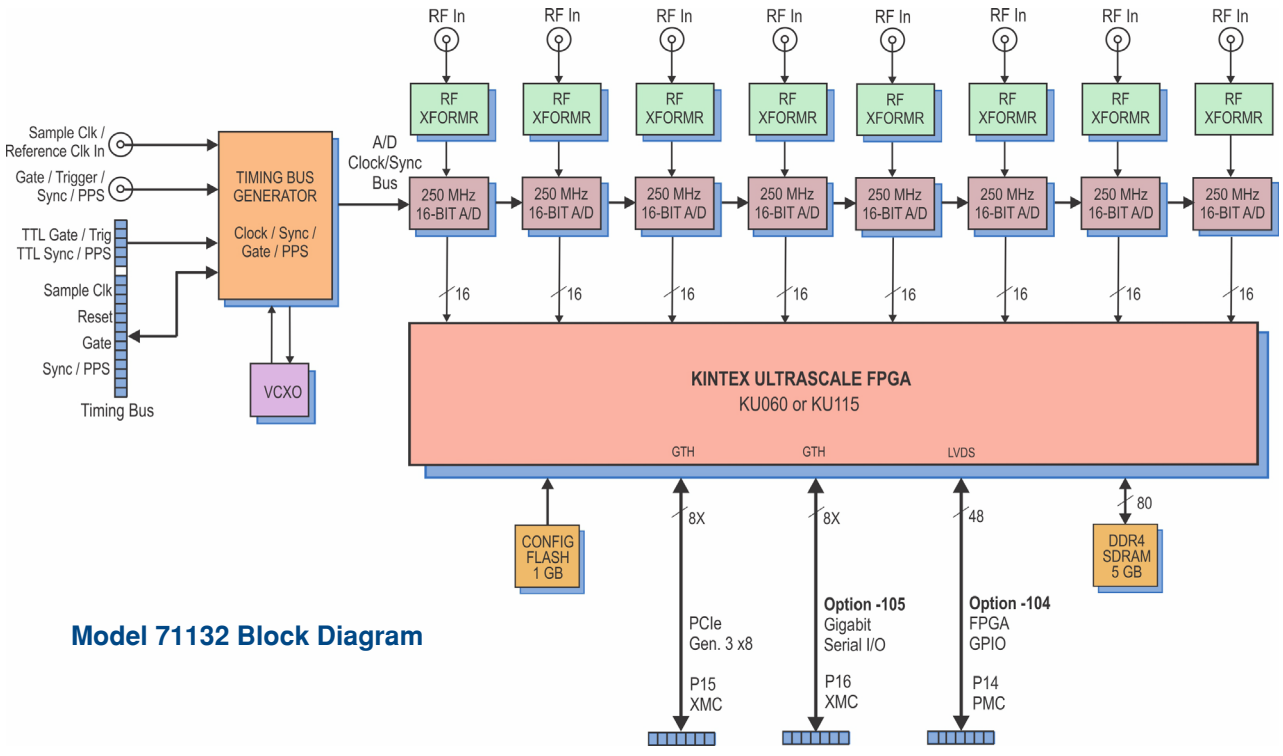
The **Pentek Jade Architecture** is based on the Xilinx Kintex UltraScale FPGA, which raises the digital signal processing (DSP) performance by more than 50% (when compared previous generation products) with equally impressive reductions in cost, power dissipation, and weight. As the central feature of the Jade Architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. A 5 GB bank of DDR4 SDRAM is available to the FPGA for custom applications. The x8 PCIe Gen 3 link can sustain 6.4 GB/s data transfers to system memory. Eight additional gigabit serial lanes and LVDS general purpose I/O lines are available for custom solutions.

Navigator Design Suite for Streamlined IP Development

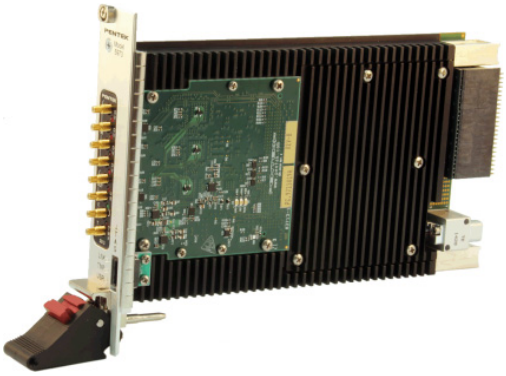
Pentek's **Navigator Design Suite** consists of two components: **Navigator FDK** (FPGA Design Kit) for integrating custom IP into Pentek sourced designs and **Navigator BSP** (Board Support Package) for creating host applications. The **Navigator FDK** includes the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

The **Navigator BSP** is a complete library of software functions for operation of the board. Each hardware and IP functional block included in the board's architecture has an associated software module for controlling that function. This one-to-one mapping between software and hardware makes writing applications for the board more intuitive and simplifies the task of updating software to control new, user created FPGA IP functions. The BSP includes a collection of sample applications and a full-featured signal analyzer tool that displays data in time and frequency domains. The Navigator BSP is available for Windows and Linux operating systems.

For more information about Model 71132, click here. For more information about the Jade family, click here. ❒



Model 71132 Block Diagram



Pentek's JadeFX™ Model 5983

Kintex UltraScale FMC Carrier for 3U VPX

Pentek recently announced the **JadeFX™ Model 5983**, a 3U VPX carrier board for FMC and FMC+ modules based on the high-performance Xilinx Kintex Ultrascale FPGA. The Model 5983 includes a VITA-57.4 FMC site providing access to a wide range of I/O options. When combined with any of Pentek's Flexor® FMCs to create a FlexorSet®, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

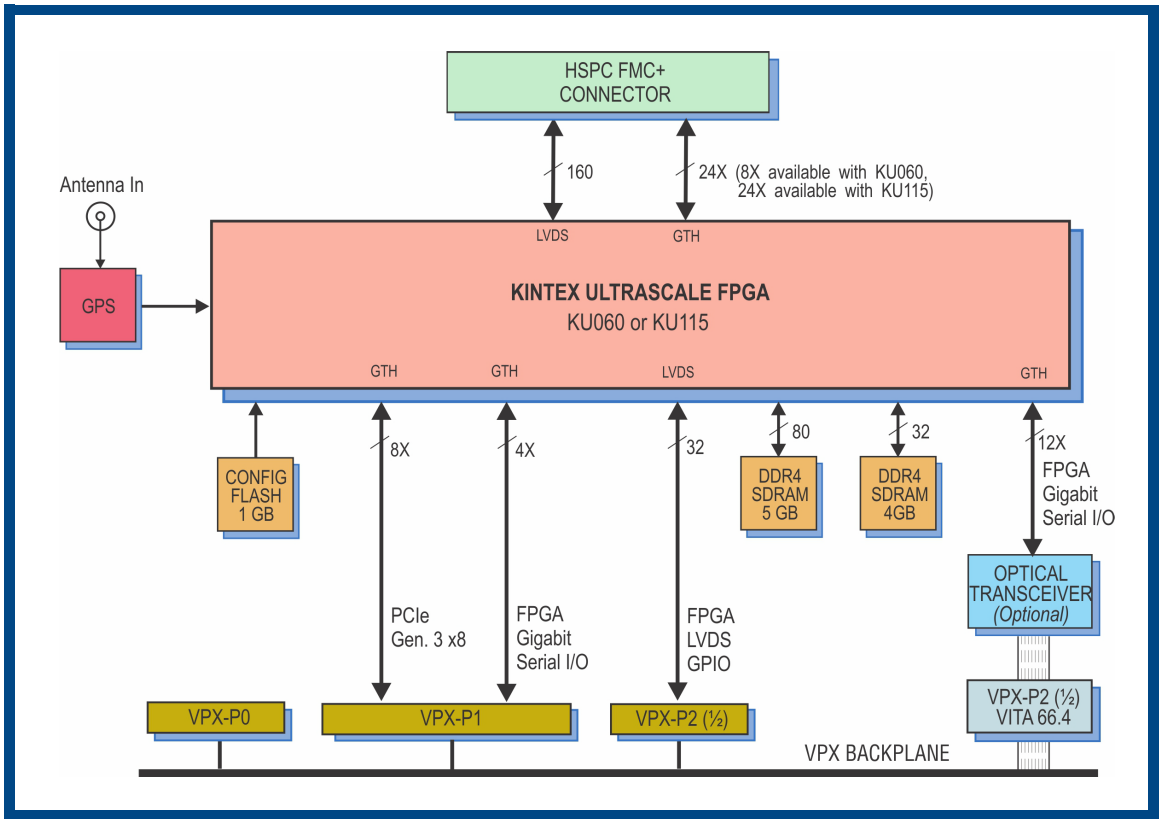
The Model 5983 is the carrier foundation for a new series of FlexorSets capable of hosting FMC and FMC+ modules. Enhancements include:

- 1.5 times higher performance using 15% less power with the Kintex Ultrascale FPGA
- 2.8 times increase in FMC bandwidth potential with the new FMC+ standard
- 9 GB of 2400 MHz DDR4 SDRAM is 2.25 times larger and 1.5 times faster
- Optional GPS for precise data tagging for time and position
- Optional 12 GB/sec VITA-66.4 optical backplane I/O
- Navigator BSP and FDK for streamlined IP development

"The Model 5983 substantially improves performance in all aspects," said Bob Sgandurra, director of Product Development of Pentek. ***"Our customers are excited to upgrade existing designs and launch new programs that can take advantage of these improvements. The Model 5983 becomes the biggest and brightest member of our FlexorSet offerings with these enhancements."***

The JadeFX Architecture for Flexor FMCs

The Pentek JadeFX Architecture defines Pentek FMC and FMC+ carrier boards based on the Xilinx Kintex UltraScale FPGA, which raises the digital signal processing (DSP) performance by 1.5 times with equally impressive reductions in cost, power dissipation, and weight. As the central feature of the JadeFX Architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. Two banks of SDRAM totaling 9 GB and operating at 2400 MHz support custom FPGA applications. The x8 PCIe Gen 3 link can sustain 6.4 GB/s data transfers to system memory.



Eight additional gigabit serial lanes and LVDS general-purpose I/O lines are available for custom solutions.

The Model 5983 supports the ANSI/VITA-66.4 optical interconnect standard that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the optical interface enables gigabit backplane communications between boards at up to 12 GB/sec independent of the PCIe interface.

FlexorSets

The **Model 5983 JadeFX carrier** is designed to operate with all of Pentek's Flexor FMC and FMC+ modules. When integrated as a **FlexorSet** package, the Model 5983 is delivered with factory-installed intellectual property (IP) modules ideally matched to the FMC's analog or digital interfaces. These include A/D acquisition and D/A waveform playback engines for simplifying data capture and playback.

The Advantages of Pentek's FlexorSets

Although Pentek's FMC modules and FMC carriers can be purchased separately, we strongly recommend purchasing our FlexorSet combinations. With **FlexorSets**, you benefit from the following:

- A full suite of board functions are included in the IP provided with the carrier
- The best analog performance is guaranteed when both the FMC carrier and FMC are designed by Pentek
- Single Pentek point of support contact for both FMC carrier and FMC module
- Completely assembled and tested board set for immediate use, right out the box, with software examples.

The table below shows Pentek's entire FlexorSet product line.

Navigator Design Suite for Streamlined IP Development

Pentek's JadeFX products are supported by Pentek's **Navigator® Design Suite**, which consists of two components: **Navigator FDK** (FPGA Design Kit) for integrating custom IP into Pentek sourced designs and **Navigator BSP** (Board Support Package) for creating host software applications. The FDK includes factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Users can work efficiently at the API level for software development and with an intuitive graphical interface for IP design. The Navigator BSP is available for Windows and Linux operating systems.

For more information about **Model 5983, click here**. You also can email us at **sales@pentek.com**, contact **your local representative**, or contact Pentek directly [+1 (201) 818-5900]. ❐

Pentek FlexorSet Models

Form Factor	FPGA Type Development Tools	Carrier Model	FMC Model	FlexorSet Model	Description
3U VPX	**Virtex-7** ReadyFlow BSP GateFlow FDK Vivado OnyxFX	5973	3312	5973-312	4 Ch 250 MHz A/D & 2 Ch 800 MHz D/A
				5973-313	As above with 4 multiband DDCs & interpolation filters
			3316	5973-316	8 Ch 250 MHz 16-bit A/D
				5973-317	As above with 8 multiband DDCs
			3320	5973-320	2 Ch 3 GHz A/D & 2 Ch 2.8 GHz MHz D/A
			3324	5973-324	4 Ch 500 MHz A/D & 4 Ch 2 GHz D/A
	Kintex UltraScale Navigator BSP Navigator FDK Vivado JADEFX	5983	3312	5983-313	4 Ch 250 MHz A/D & 2 Ch 800 MHz D/A with 4 multiband DDCs & interpolation filters
			3316	5983-317	8 Ch 250 MHz 16-bit A/D with 8 multiband DDCs
			3320	5983-320	2 Ch 3 GHz A/D & 2 Ch 2.8 GHz MHz D/A
			3324	5983-324	4 Ch 500 MHz A/D & 4 Ch 2 GHz D/A
PCIe	**Virtex-7** ReadyFlow BSP GateFlow FDK Vivado OnyxFX	7070	3312	7070-312	4 Ch 250 MHz A/D & 2 Ch 800 MHz D/A
				7070-313	As above with 4 multiband DDCs & interpolation filters
			3316	7070-316	8 Ch 250 MHz 16-bit A/D
				7070-317	As above with 8 multiband DDCs
			3320	7070-320	2 Ch 3 GHz A/D & 2 Ch 2.8 GHz MHz D/A
			3324	7070-324	4 Ch 500 MHz A/D & 4 Ch 2 GHz D/A

JADE vs. JADEFX: What's the difference?

Pentek's JADE Architecture

- Xilinx Kintex UltraScale FPGA
- Navigator Design Suite Software
- Powerful linked-list DMA engines
- 2400 MHz DDR4 SDRAMs
- PCIe Gen.3 x8 for control and data-transfer
- I/O to support a wide range of signal types
- Secondary copper & optical serial gigabit I/O
- On-board clocking and synchronization
- VPX products compatible with VITA-46, VITA-48, and VITA-65 OpenVPX
- Commercial and several ruggedization levels support both air and conduction cooling

- 5520 DSP Slices
- 1.15 Million Gates
- Lower cost
- Lower power
- Faster memory and I/O

Two Pentek product families sharing the Jade Architecture

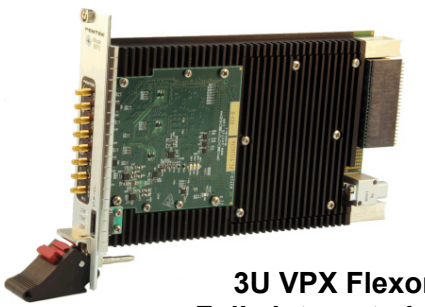
JADE Products

- XMC module based
- Form Factors: XMC,PCIe, 3U & 6U VPX, AMC, 3U & 6U cPCI
- 8 GB/sec gigabit serial optical I/O
- 4 GB DDR4 SDRAM

JADEFX Products

- FMC module based
- 3U VPX FMC Carrier
- VITA 57.4 FMC+ site
- VITA 66.4 12 GB/sec gigabit serial optical backplane I/O
- 9 GB DDR4 SDRAM

XMC **3U VPX** **6U VPX** **PCIe**



3U VPX FlexorSet: Fully integrated JadeFX carrier plus FMC module

Product Focus

Talon Rugged Small Form Factor RF/IF Recorders Optimized for SWaP

TALON RTR RUGGED RECORDER

Pentek recently announced a new **Talon RTR** series: a high-performance small form factor (SFF) recorder product line for analog IF/RF signals. Optimized for SWaP (size, weight and power), the Pentek Talon RTR SFF recorders provide levels of performance and storage capacity previously only possible in much larger rack-mountable products. Measuring 5.25" H x 8.5" W x 14" D and weighing only 17 pounds, this small package is capable of sustained real-time recording speeds up to 4 GB/s and can hold up to 30.7 TB of removable SSD storage. Power consumption has been greatly reduced, with most systems drawing less than 120 W at full operation.

The Talon RTR SFF product line offers a variety of RF/IF I/O modules, providing multi-channel, wide-bandwidth RF recording with A/D sample rates ranging from 200 MS/sec to 3.6 GS/sec. An integrated high-speed RAID controller is coupled with enterprise class SSDs for hours of real-time, wide bandwidth data capture.

Up to eight hot-swap SSDs deliver a total storage capacity of up to 30.7 TB with support for RAID levels 0, 5, or 6. All eight SSD data drives and the single operating system SSD can be easily removed in seconds from front panel drive bays. Drives are mounted on sleds for easy transfer to an offload system so the recorder can remain installed while data is transported to the lab.

Ease of Operation

Talon recorders are built on a Windows OS with an Intel Core i7 processor and provide both a Windows-based GUI and API to control the system. All Talon RTR SFF recorders include Pentek's SystemFlow® software which includes signal viewing and analysis tools so the user can monitor input signals signal before, during, and after a recording session. These tools include a virtual oscilloscope, spectrum analyzer, and spectrogram displays. SystemFlow provides point-and-click configuration management and storage of custom configurations for single-click setup. A user API allows custom recorder control interfaces to be easily built. Users can install post-processing and analysis tools to operate on the data that is saved to the native NTFS file system.

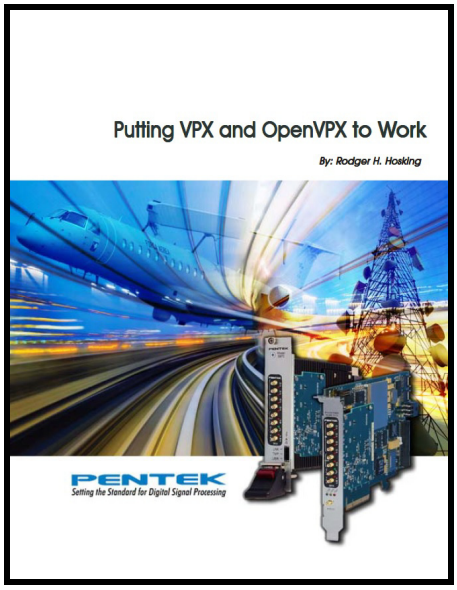
Available Models & Options

The Talon RTR SFF recorders offer an optional GPS receiver for precise time and position stamping. An ATX power supply accepts 110V-240V AC, drawing under 150W and typically around 100W. Models have options for a 6-30 VDC power supply and a removable operating system drive. Several options for RF/IF analog inputs are available. I/O on all models includes USB 2.0, 3.0, and 3.1 ports and dual Gigabit Ethernet connections. Following are the available models:

- Model 2546: 200 MS/sec SFF Recorder
- Model 2547: 500 MS/sec SFF Recorder
- Model 2548: 1 GS/sec SFF Recorder
- Model 2549: 3.6 GS/sec Ultra Wideband SFF Recorder

Each list item above is linked to further information. ❐

Resources Relevant to this Issue of Pipeline (click image to download)



Putting VPX and OpenVPX to Work

Jade Kintex UltraScale FPGA Brochure

Join Us at Your Desktop for a Webcast!

Leveraging New Embedded Systems Standards for EW, SIGINT, and Radar Applications

Presented by Rodger Hosking

April 17, 2018 - 11 AM to 12 PM ET

As enemy threats become more complicated and sophisticated, there is within the Department of Defense (DoD) a demand for advanced RF and microwave solutions to counter those threats. Spectrum dominance, electronic warfare (EW), radar upgrades, and other sensor applications require system designers to leverage multi-function, multi-platform systems while also reducing size, weight, and power (SWaP) throughout these systems. This webcast will discuss how emerging standards help meet the challenges of platform flexibility, reusability of hardware and software, quick reaction to new threats, and insertion of new technology. Click **here** to register.

SDR Techniques to Handle Complex and Jam–Packed Spectral Landscapes

Presented by Rodger Hosking

May 15, 2018 - 2 PM to 3 PM ET

Demand is at an all-time high for advanced communications systems and components that support simultaneous, reliable, and secure voice, video, and data sharing. However, systems engineers and integrators, as well as end users, face a growing number of requirements and challenges. This webcast will discuss the value of software-defined radios in the design, development, prototyping, and testing of communications systems that address: the increasingly congested, complex spectrum environment; heterogeneous networks; interoperability and compatibility; hardware and software integration; and security and transmission requirements and standards. Click **here** to register.

Or in Oklahoma City at the 2018 IEEE Radar Conference!

April 23 - 27 2018

This conference will be a continuation of the annual IEEE radar series (formerly the IEEE National Radar conference). These conferences cover the many disciplines that span the applications of modern radar systems, including systems-level through subsystem and component technologies, antennas, and signal processing (deterministic and adaptive). The scope includes systems architectures of monostatic, bistatic and multistatic, and ground-based, airborne, shipborne, and spaceborne realizations.

Renaissance Oklahoma City
Convention Center Hotel
10 North Broadway Avenue
Oklahoma City, OK, USA

www.radarconf18.org