16-Channel Multiband Receiver with A/Ds and FPGA - PCI

Features

- Two 80 or 105 MHz, 14-bit A/D converters
- 16 channels of multiband digital downconverters
- 5 kHz to 10 MHz output bandwidth for f_S = 100 MHz
- 250 MHz input bandwidth
- Ideal for IF sampling
- User-configurable Xilinx Virtex-II FPGA
- Custom FPGA I/O through a 64-pin DIN connector
- Bypass path allows direct capture of A/D data
- Front panel clock and sync bus
- Synchronization of up to 80 modules (with Model 9190)

General Information

Model 7631 is a half-length PCI multi-band receiver. It consists of one Model 7131 receiver mounted on a PCI carrier board. The Model 7631 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

Front End

The Model 7631 accepts two analog RF inputs at +4 dBm full scale into 50 ohms on PCI slot panel SMA connectors.

The two inputs are transformer coupled and digitized by AD6645 14-bit A/D converters. The AD6645 operates at a maximum sampling rate of 80 MHz in the standard unit and up to 105 MHz with option -100.

The sampling clock can be driven from an internal 80 MHz or 100 MHz crystal oscillator, or from an external sample clock supplied through a PCI slot panel SMA connector or the PCI slot panel sync bus.

Digital Downconverters

The 7631 includes four TI/Graychip GC4016 quad multiband digital downconverter chips. The maximum input sampling rate for the GC4016 is 100 MHz. Each device includes four independently tunable channels capable of center frequency tuning from DC to $f_S/2$, where f_S is the sample clock frequency.

Each GC4016 accepts two 14-bit parallel inputs from the two A/D converters. A cross-bar switch in each GC4016 allows all 16 channels on the board to select either of the two A/D inputs for flexible switching.

Output Bandwidth

With a 100 MHz sample clock, the useable output bandwidth of each of the downconverter channels is 2.5 MHz. However, since these models deliver parallel digital outputs from the GC4016 into the FPGA, users can take advantage of the GC4016 channel combining mode to join two or four channels into a single channel with a resulting bandwidth of 5 or 10 MHz, respectively. This supports many of the new wideband wireless standards.

Since both A/D converters connect directly to the FPGAs, signals with even wider bandwidths can be accommodated.
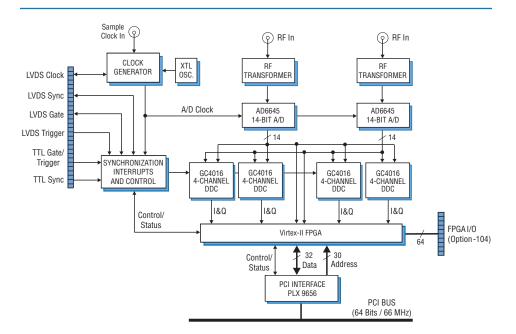
FPGA

The downconverter outputs are delivered to a Xilinx Virtex-II XC2V3000 FPGA which is factory configured to perform various modes of data packing, formatting and channel selection.

Dual port memories in the FPGA provide efficient PCI Bus transfers by buffering downconverter and A/D data.

The A/D outputs are also connected directly to the FPGA so that wideband A/D data can be delivered directly to the baseboard bypassing the downconverters. An A/D decimation mode allows one of every N samples to be written into the FPGA memory, where N is any integer between 1 and 4096. This overcomes the lower frequency limit on the A/D sample clock.

Option -104 installs 64 signal line connections to the XC2V3000 FPGA for custom I/O through a 64-pin DIN connector. ➤

➤ Synchronization

The front panel clock and sync bus allow one 7631 to act as a master, driving the sample clock out to a front panel cable bus using LVDS differential signaling.

Additional sync lines on the bus allow synchronization of the local oscillator phase, frequency switching, decimating filter phase, and data collection on multiple 7631's.

Up to eight slave 7631 boards can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 boards may be synchronized with a Model 9190 Clock and Sync Generator. In addition to the LVDS timing bus, the Model 7631 can receive front panel TTL external signals for gate and trigger functions .

Interrupt Sources

The Model 7631 has several maskable interrupt sources. PCI interrupts may be generated by A/D converter overload output codes, transitions on the gate signals, clock loss, buffer swapping, a programmable over-temperature condition or faulty power supply voltage.

The ADM1024 Voltage/Temperature Monitor provides constant monitoring of critical voltages and temperatures and generates an interrupt if values exceed threshold limits which are user-programmable over the PCI interface.

PCI Interface

The FPGA output is connected to a 66 MHz, 64-bit PCI interface capable of 528 MB/sec peak data rates. An industry standard PLX9656 PCI interface chip ensures full conformance to all PCI bus timing specifications.

Specifications

Front Panel Analog Signal Inputs
   Input Type: Transformer-coupled, front panel female SMA connectors
   Transformer Type: Mini-Circuits ADT4-6T
   Full Scale Input: +4 dBm into 50 ohms
   3 dB Passband: 60 kHz to 270 MHz

A/D Converters, Standard
   Type: Analog Devices AD6645-80
   Sampling Rate: 30 MHz to 80 MHz
   Internal Clock: 80 MHz crystal osc.
   External Clock: 30 to 80 MHz
   Resolution: 14 bits
A/D Converters, Option -100
   Type: Analog Devices AD6645-105
   Sampling Rate: 30 MHz to 105 MHz
   Internal Clock: 100 MHz crystal osc.
   External Clock: 30 to 105 MHz
   Resolution: 14 bits
Clock Source: Onboard crystal oscillator, front panel ext clock, or LVDS clock
External Clock
   Type: Front panel female SMA connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms impedance
Sync/Gate Bus
   Type: 26-pin connector, with one clock, one sync, and two gate input/output LVDS signals; two trigger LVDS inputs; and one sync and one gate input TTL signals
Digital Downconverters
   Type: TI/Graychip GC4016
   Decimation: 32 to 16,384; with channel combining mode: 8 or 16
   Data Source: A/D outputs are connected to all GC4016's
   Output: Parallel complex data
Bypass Mode: Data from the A/D converters can be written directly into the FPGAs at a sample rate equal to the A/D clock decimated by any integer between 1 and 4096
Field Programmable Gate Array
   Option -300: Virtex-II XC2V3000
   Option -104: Installs 64-pin DIN connector with 64 lines to the XC2V3000 FPGA
Dual Port RAM Data Buffers
   Size: 8k x 32 DPRAM
PCI Interface
   Type: PLX Technology PCI 9656
   PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)
   Local Bus (FPGA): 32-bit, 66 MHz
   Data Transfer Modes: Direct slave mode and DMA mode
PCI Bridge: 64-bit, 66 MHz
Environmental:
   Operating Temp: 0° to 50° C
   Storage Temp: –20° to 90° C
   Relative Humidity: 0 to 95%, non-cond.
Size: Standard PCI half-length board

Ordering Information

Model	Description
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Options:

-100	105 MHz A/D with 100 MHz oscillator
-104	64-pin DIN connector with FPGA I/O
-300	XC2V3000 FPGA