New!

Models 57741 & 58741

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGAs - 6U OpenVPX

Model 58741

General Information

Models 57741and 58741 are members of the Onyx® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71741 XMC modules mounted on a VPX carrier board.

Model 57741 is a 6U board with one Model 71741 module while the Model 58741 is a 6U board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters, four or eight banks of memory, and one or two wideband DDCs.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules and one or two wideband DDCs. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

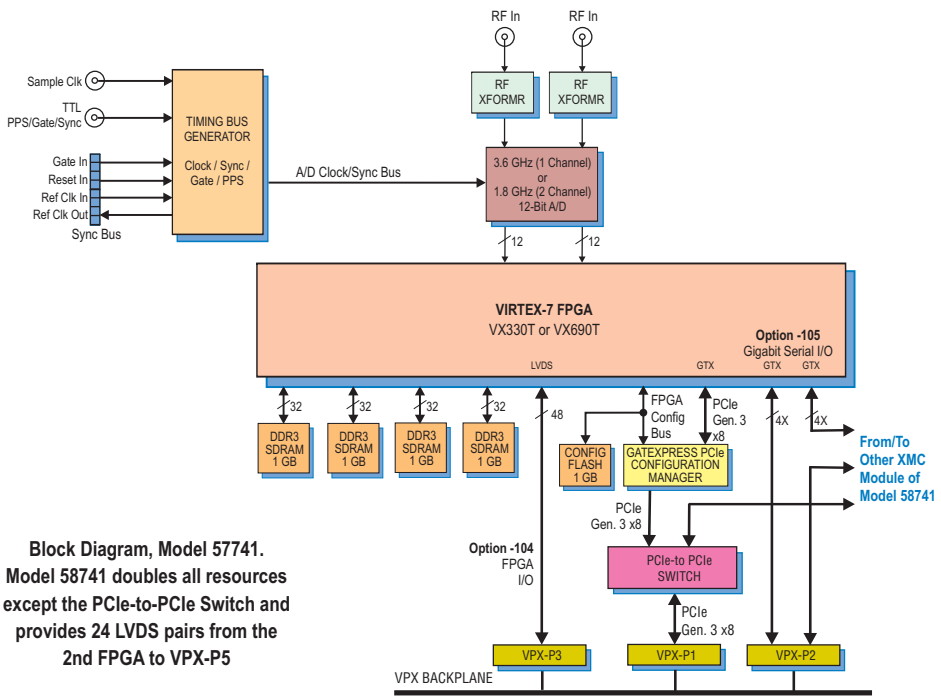
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57741; P3 and P5, Model 58741.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57741; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58741. ➤

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One or two 1-channel mode with 3.6 GHz, 12-bit A/Ds
- Two or four 2-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDCs (Digital Downconverters)
- 4 or 8 GB of DDR3 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57741. Model 58741 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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A/D Acquisition IP Module

These models feature two or four A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or a test signal generator. The IP modules have associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, four banks are used to store the single-channel of input data. In dual-channel mode, two memory banks store data from input channel 1 and two memory banks store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Core

Within each FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

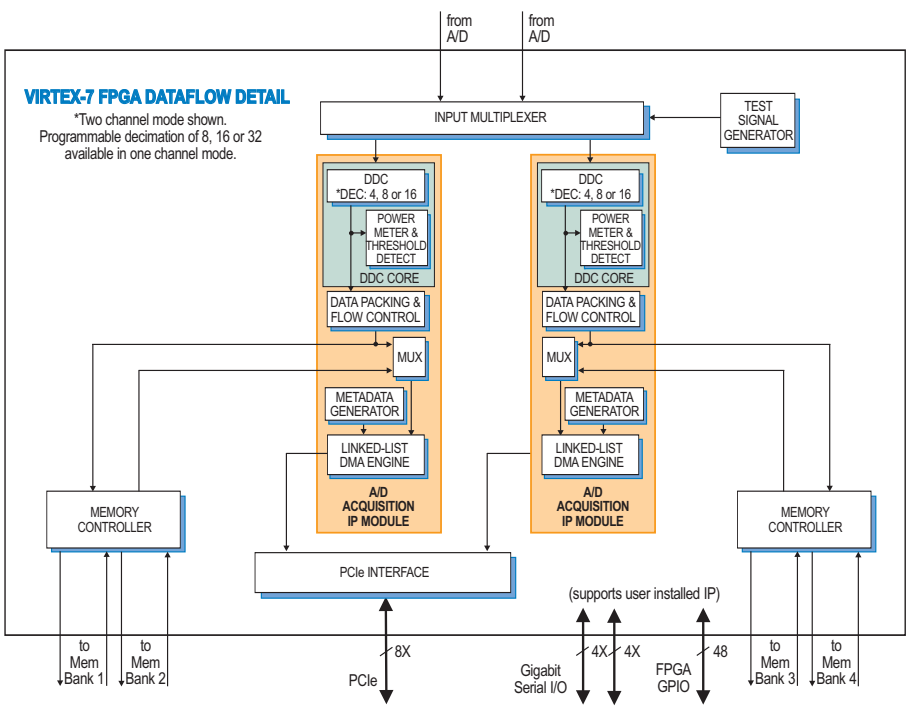
➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it's programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed. ➤



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Memory Resources

The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Ordering Information

Model	Description
57741	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-7 FPGA - 6U VPX
58741	2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, two Virtex-7 FPGAs - 6U VPX
Options:	
-076	XC7VX690T-2 FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57741; P3 and P5 connectors, Model 58741
-105	Gigabit link between the FPGA and P2 connector, Model 57741; gigabit links from each FPGA to P2 connector, Model 78741

Contact Pentek for availability of rugged and conduction-cooled versions

➤ The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx iMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

A/D Converter Stages

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing these models to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two boards can be synchronized with a simple cable. For larger systems, multiple boards can be synchronized using the Model 5292 high-speed sync board to drive the sync bus.

Specifications

Model 57741: One A/D
Model 58741: Two A/Ds
Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converters (1 or 2)
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable
Digital Downconverters (2 or 4)
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Sample Clock Sources (1 or 2)
Front panel SSMC connector
Timing Bus (1 or 2)
19-pin µSync bus connector includes sync and gate/trigger inputs, CML
External Trigger Input (1 or2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2
Custom I/O
Option -104: Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57741; P3 and P5, Model 58741
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57741; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58741.
Memory Banks (4 or 8)
Type: DDR3 SDRAM
Size: 1 GB each
Speed: 800 MHz (1600 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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