New!

4- or 8-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 6U OpenVPX

Model 58671

Features

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 1.25 GHz 16-bit D/As
- Four or eight digital upconverters
- Extended interpolation range from 2x to 1,048,576x
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 or 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- Dual-or Quad μSync clock/ sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Models 57671 and 58671 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71671 XMC modules mounted on a VPX carrier board.

Model 57671 is a 6U board with one Model 71671 module while the Model 58671 is a 6U board with two XMC modules rather than one.

These models include four or eight D/As with a wide range of programmable interpolation factors, four or eight DUCs, and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include four or eight D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, test signal generators,

and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.
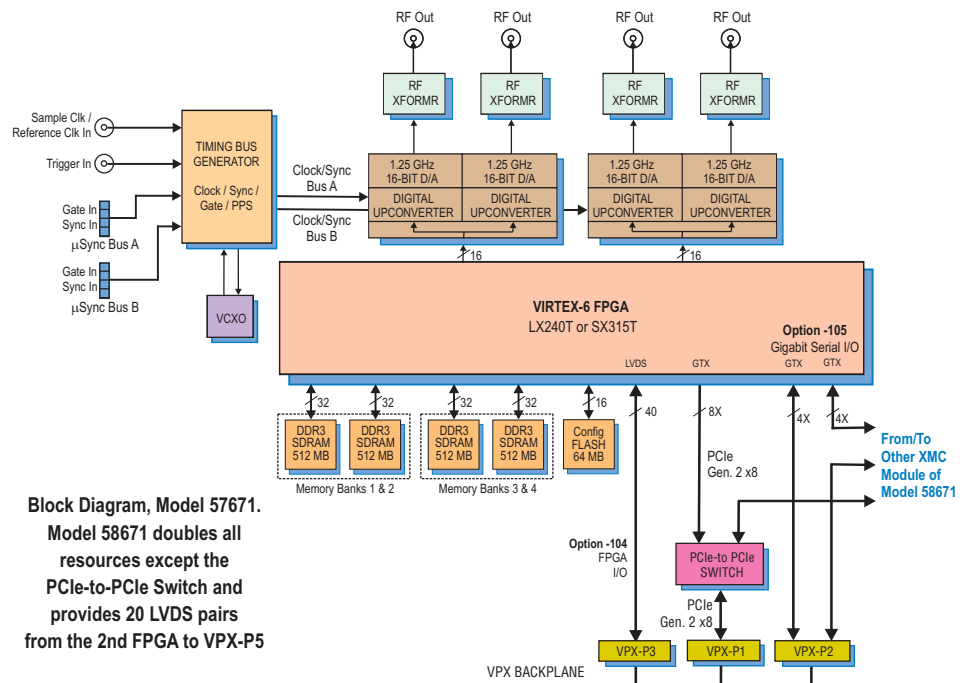
Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57671; P3 and P5, Model 58671.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57671; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58671. ➤

Block Diagram, Model 57671. Model 58671 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

➤ Digital Upconverter and D/A Stage

Two or four Texas Instruments DAC3484s provide four or eight DUCs (digital upconverters) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGAs and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, these models feature an FPGA-based interpolation engine which adds two additonal interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog outputs are through front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Model 9192 Cobalt Synchronizers can drive multiple µSync connectors enabling large, multichannel synchronous configurations.

Memory Resources

The architecture of these models supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤
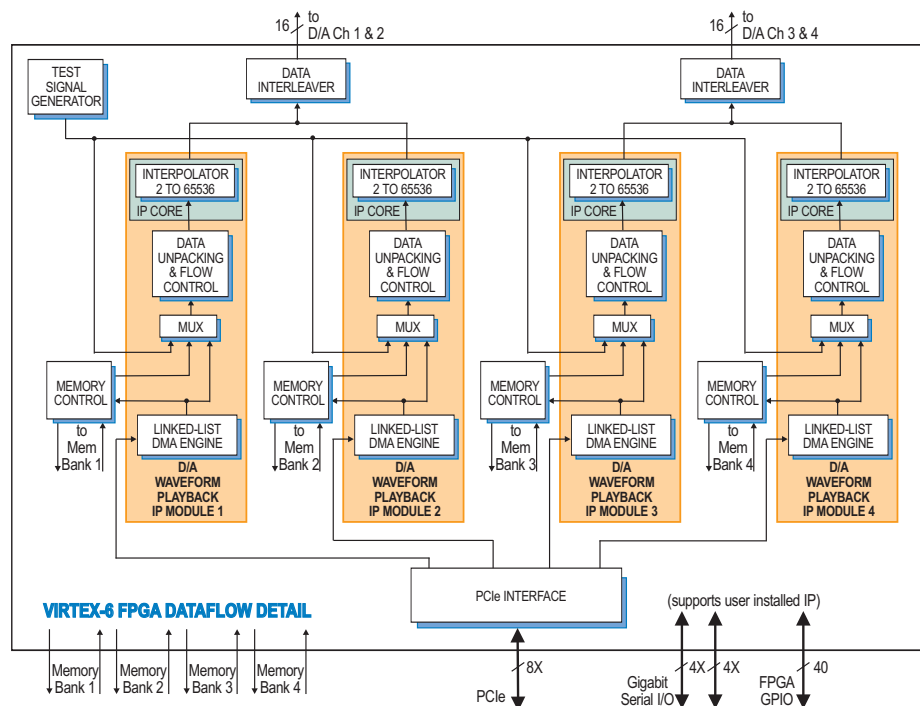
D/A Waveform Playback IP Module

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. Four or eight linked-list controllers support waveform generation to the four or eight D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4, as well as to the other four channels of Model 58671.

Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 or 128 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.

VIRTEX-6 FPGA DATAFLOW DETAIL

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➤ PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57671: 4-Channel DUC, 4-channel D/A

Model 58671: 8-Channel DUC, 8-channel D/A

D/A Converters (4 or8)
  Type: TI DAC3484
  Input Data Rate: 312.5 MHz max.
  Output Bandwidth: 250 MHz max.
  Output Sampling Rate: 1.25 GHz max. with interpolation
  Interpolation: 2x, 4x, 8x or 16x
  Resolution: 16 bits

Digital Interpolator
  Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Front Panel Analog Signal Outputs (4 or 8)
  Output Type: Transformer-coupled, front panel female SSMC connectors
  Full Scale Output: Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
  Full Scale Output Programming: $1.0x(G+1)/16$ Vp-p, where 4-bit integer $G = 0$ to 15

Clock Synthesizers (1 or 2)
  Clock Source: Selectable from on-board programmable VCXO or front panel external clock
  VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
  Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
  Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clocks (1 or 2)
  Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Inputs (1 or 2)
  Type: Front panel female SSMC connector
  Function: Programmable functions include: trigger, gate, sync and PPS

Timing Bus (1 or 2): 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Arrays (1 or 2)
  Standard: Xilinx Virtex-6 XC6VLX240T-2
  Optional: Xilinx Virtex- 6 XC6VSX315T-2

Custom I/O
  Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57671; P3 and P5, Model 58671
  Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57671; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58671

Memory Banks (1 or 2)
  Four or eight 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
  PCI Express Bus: Gen. 1 or 2: x4 or x8

Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
57671	4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 6U VPX
58671	8-Channel 1.25 GHz D/A with DUC, Extended Interpolation and two Virtex-6 FPGAs - 6U VPX

Options:

-002*	-2 FPGA speed grade
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57671; P3 and P5 connectors, Model 58671
-105	Gigabit link between the FPGA and P2 connector, Model 57671; gigabit links from each FPGA to P2 connector, Model 58671
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions