

New!

# Models 57641 & 58641

# 1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - 6U OpenVPX



Model 58641



## General Information

Models 57641 and 58641 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71641 XMC modules mounted on a VPX carrier board.

Model 57641 is a 6U board with one Model 71641 module while the Model 58641 is a 6U board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters, one- or two-channel programmable digital downconverters, and four or eight banks of memory.

## The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules and one or two wideband DDCs. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchro-

nization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57641; P3 and P5, Model 58641.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57641; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58641.

## A/D Converter Stage

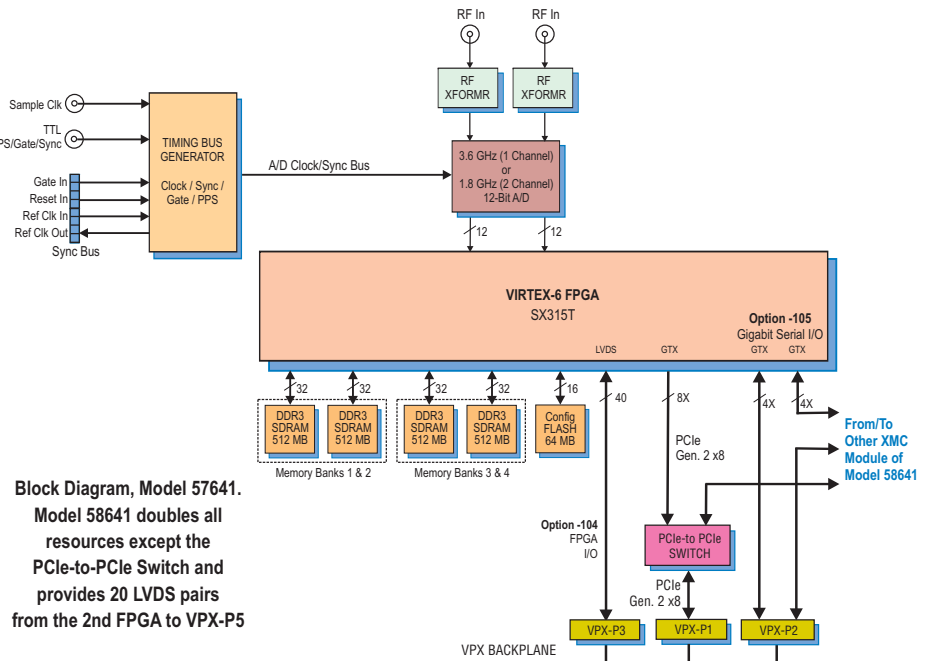
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources. ➤

## Features

- Ideal radar and software radio interface solution
- One or two 1-channel mode with 3.6 GHz, 12-bit A/Ds
- Two or four 2-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDCs (Digital Downconverters)
- 2 or 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- μSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



**A/D Acquisition IP Modules**

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or a test signal generator. The IP modules have associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

**DDC IP Cores**

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to  $f_s$ , where  $f_s$  is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of  $0.8 * f_s / N$ , where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of  $f_s / N$ .

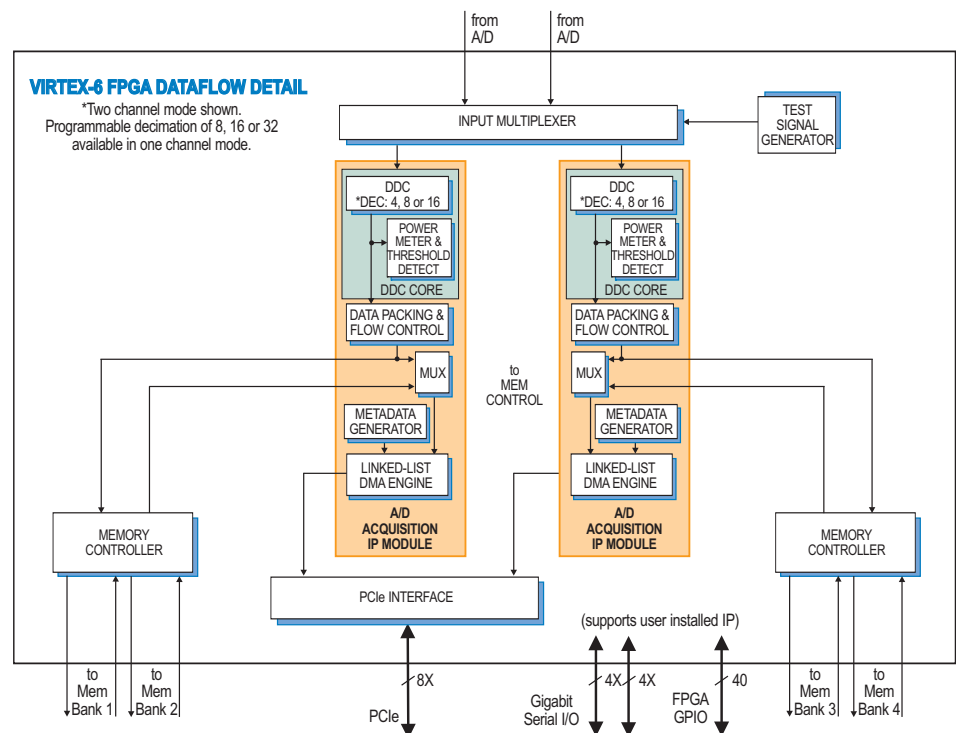
**Clocking and Synchronization**

These models accept a 1.8 GHz dual-edge sample clock via front panel SSMC connectors. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple boards can be synchronized using the Cobalt high-speed sync board to drive the sync bus.

**Memory Resources**

The Cobalt architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer. ➤



► **PCI Express Interface**

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Specifications**

**Model 57641: One A/D**

**Model 58641: Two A/Ds**

**Front Panel Analog Signal Inputs (2 or 4)**

**Input Type:** Transformer-coupled, front panel female SSMC connectors

**A/D Converters (1 or 2)**

**Type:** Texas Instruments ADC12D1800

**Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz

**Resolution:** 12 bits

**Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz

**Full Scale Input:** +2 dBm to +4 dBm, programmable

**Digital Downconverters (2 or 4)**

**Modes:** One or two channels, programmable

**Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz

**Decimation Range:** One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x

**LO Tuning Freq. Resolution:** 32 bits, 0 to  $f_s$

**LO SFDR:** >120 dB

**Phase Offset Resolution:** 32 bits, 0 to 360 degrees

**FIR Filter:** User-programmable 18-bit coefficients

**Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**Sample Clock Sources (1 or 2)**

Front panel SSMC connector

**Sync Bus (1 or 2)**

Multi-pin connectors, bus includes gate, reset and in and out ref clock

**External Trigger Input (1 or 2)**

**Type:** Front panel female SSMC connector, TTL

**Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Arrays (1 or 2)**

Xilinx Virtex-6 XC6VSX315T-2

**Custom I/O**

**Option -104:** Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57641; P3 and P5, Model 58641

**Option -105:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57641; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58641

**Memory Banks (1 or 2)**

Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**

**PCI Express Bus:** Gen. 1 or 2: x4 or x8

**Environmental:** Level L1 & L2 air-cooled;

Level L3 ruggedized, conduction-cooled

**Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

**Ordering Information**

Model	Description
57641	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-6 FPGA - 6U VPX
58641	2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, two Virtex-6 FPGAs - 6U VPX

**Options:**

-002*	-2 FPGA speed grade
-064*	XC6VSX315T
-104	LVDS I/O between the FPGA and P3 connector, Model 57641; P3 and P5 connectors, Model 58641
-105	Gigabit link between the FPGA and P2 connector, Model 57641; gigabit links from each FPGA to P2 connector, Model 78641
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

\* These options are always required

*Contact Pentek for availability of rugged and conduction-cooled versions*