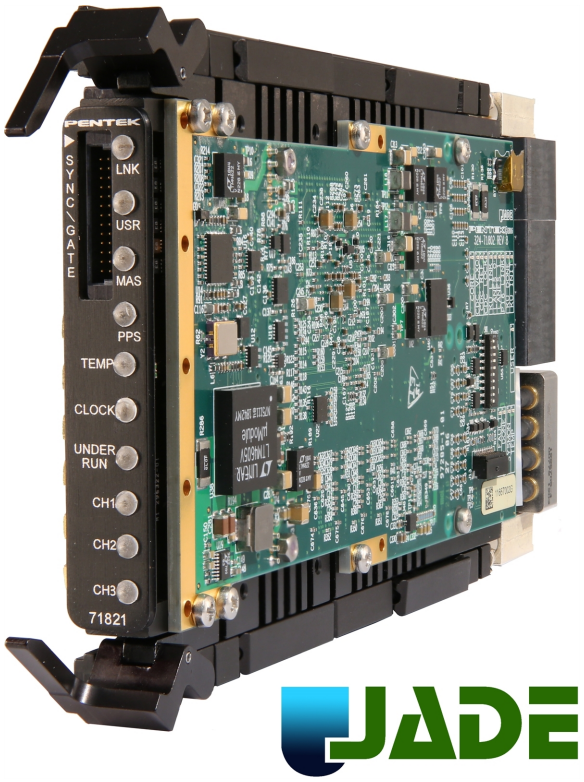
Model 54821	3-Channel 200 MHz A/D with DDC, 2-Channel 800 MHz D/A with DUC	Kintex UltraScale FPGA	3U VPX Board

Features

- Exceptional dynamic range and analog signal integrity
- Xilinx® Kintex® UltraScale™ FPGA
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of 2400 MHz DDR4 SDRAM
- Programmable frequency synthesized sample clock generator
- Sample clock synchronization to an an external reference
- Powerful DMA controllers for moving data
- PCI Express interface (Gen. 1, 2 & 3) up to x8
- Multichannel, multiboard synchronization with clock/sync bus
- Optional clock/sync generator for multiboard systems
- Optional LVDS port and gigabit serial connections for custom FPGA I/O
- Compatible with several VITA standards including: VITA 66.5, VITA 67.2, VITA 67.3C and VITA 65
- Ruggedized and conduction-cooled versions
- Navigator® BSP for software development
- Navigator® FDK for custom IP development
- Free lifetime applications support



JADE

Applications

- Complete radar and software radio interface solution
- Communication receiver and transmitter
- Radar receiver and transmitter
- Electronic Warfare transponder
- Waveform signal generator
- Analog I/O for digital recording and playback
- Wideband data acquisition
- Remote monitoring
- Sensor interfaces

The Jade Architecture

Evolved from the proven designs of Pentek's Cobalt® and Onyx® families, Jade® raises the processing performance while lowering the overall power requirements by building on the Xilinx family of Kintex UltraScale FPGAs. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions as well as providing an ideal platform for user-created intellectual property (IP).

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 54821 factory-installed functions include three A/D acquisition modules for simplifying data capture and tagging, a D/A waveform generator IP module outputting user-created waveforms, and a set of specialized DMA engines for efficient data transfers between the board and a host computer.

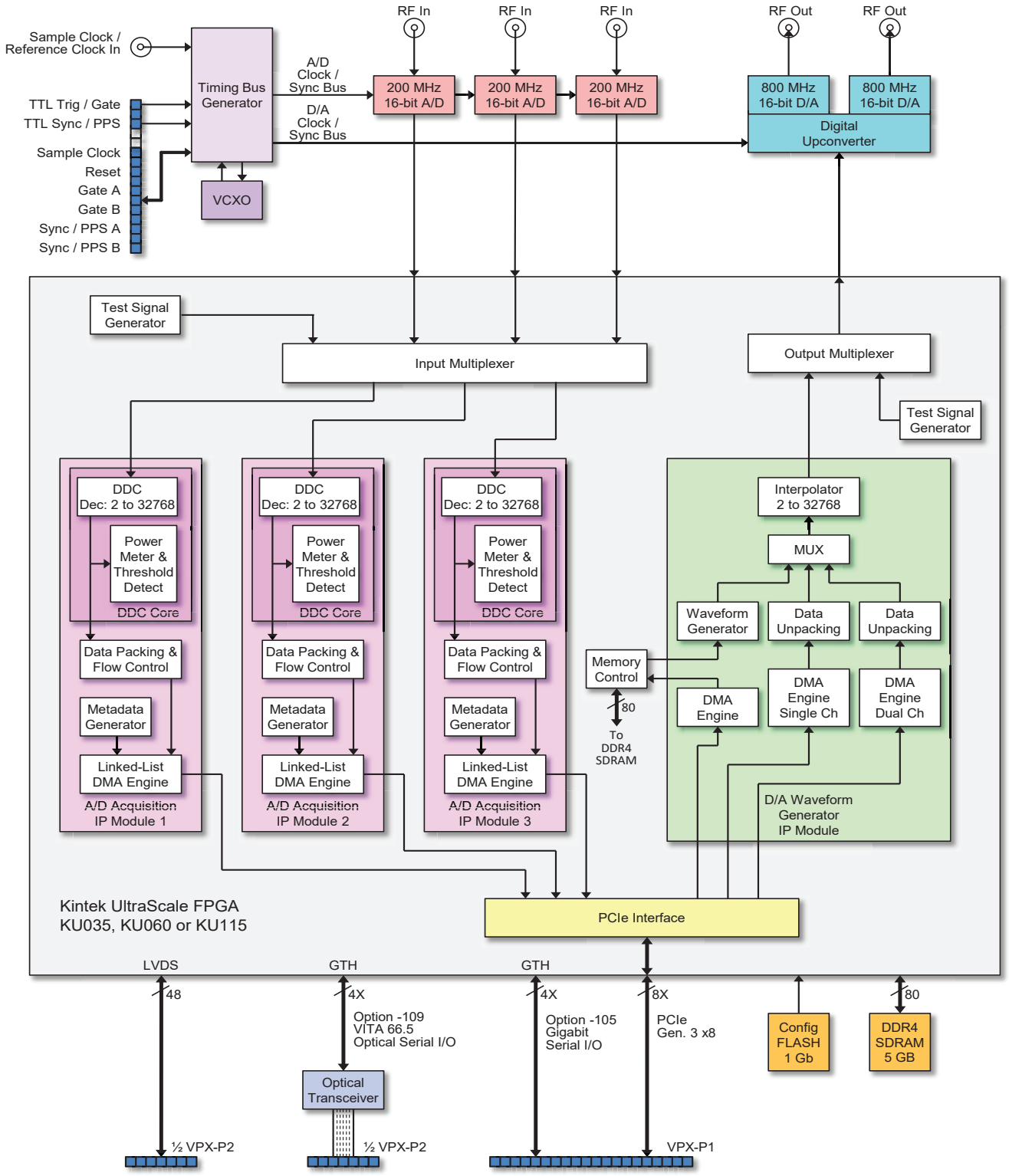
Additional IP includes: three powerful, programmable DDC IP cores; an IP module for DDR4 SDRAM memory control; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These factory-installed applications enable the 54821 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Xilinx Kintex UltraScale FPGAs

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs: KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

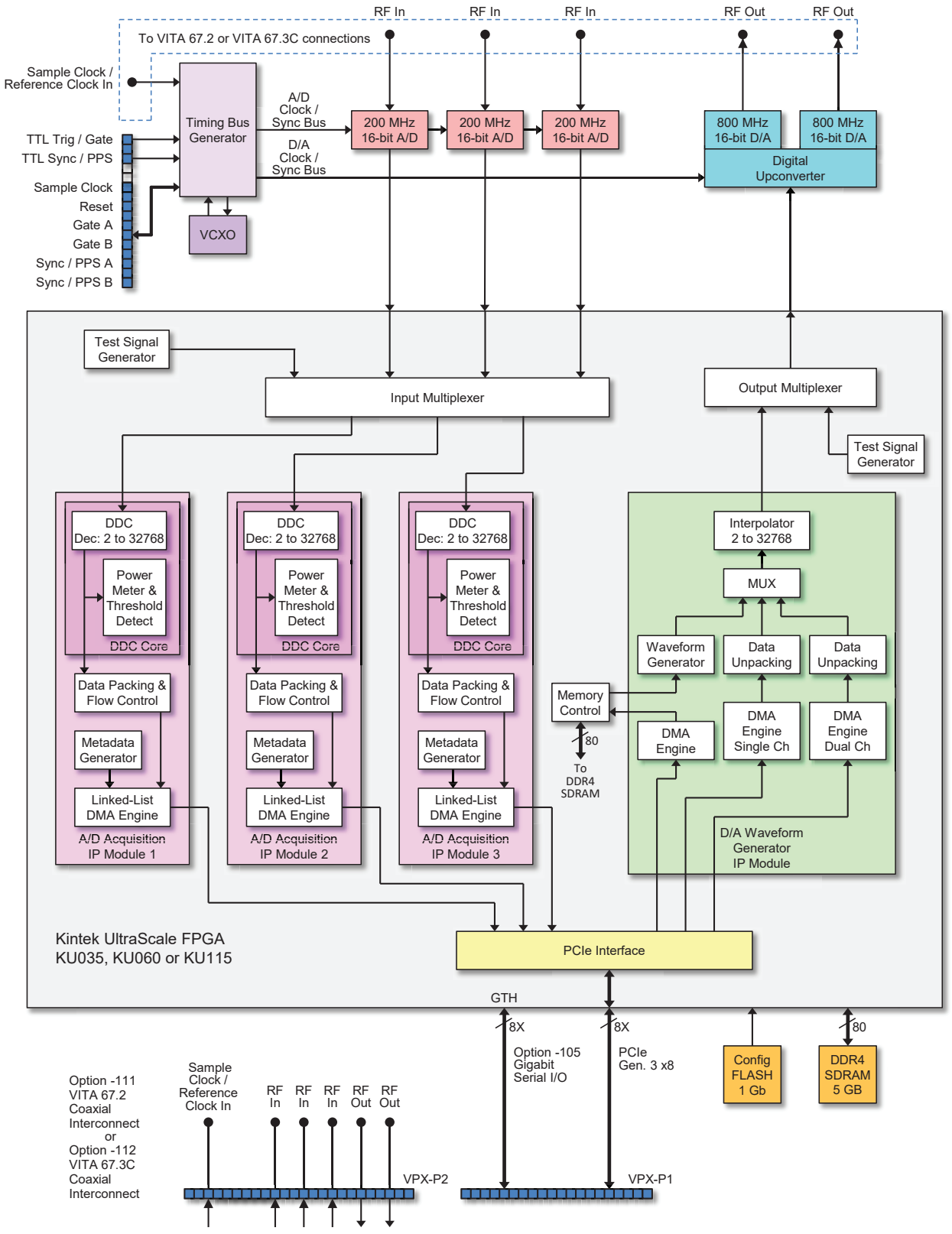
54821 Block Diagram (Standard configuration and option -109 shown.)

Click on a block for more information.



54821 Block Diagram (Options -111 and -112 shown.)

Click on a block for more information.



A/D Converter Stage

The board's analog interface accepts three analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the FPGA for signal processing, data capture, and for routing to other module resources.

A/D Acquisition IP Modules

The 54821 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, or a test signal generator. Each acquisition module has a DMA engine for efficiently moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved, including one A/D driving all DDCs or each of the A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_S, where f_S is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 32,768, providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_S/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of f_S/N.

D/A Waveform Playback IP Module

The Model 54821 factory-installed functions include a sophisticated D/A Waveform Generator IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters such as location of waveform to be output, length of waveform, and delay from playback trigger, can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

Digital Upconverter and D/A Stage

These models feature one or two Texas Instruments DAC5688s. The DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate, and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sample rate. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of transformer coupled front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes, the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths. Each timing bus includes a clock, sync, and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector.

This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules. Multiple 54821s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

For systems requiring high-channel counts, Model 9193 System Synchronization and Distribution board can synchronize up to eight 54821s.

Memory Resources

The 54821 architecture includes a 5 GB bank of DDR4 SDRAM memory. This resource is used by the board's built-in functions for data storage and buffering, but can also be used for custom applications. The Navigator FDK provides a memory controller as well as guidance on the most efficient use of the memory when creating IP functions.

PCI Express Interface

The 54821 includes an industry standard interface fully compliant with PCI Express Gen. 1, 2, and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

3U VPX Interface

The 54821 complies with the VITA 65.0 3U VPX specification. In addition to supporting PCIe Gen. 3, x8 on the VPX P1 connector, option -105 adds up to 8 more gigabit serial lanes connected directly to the FPGA for supporting user-installed protocols.

The 54821 offers flexible analog and digital interface options for the VPX-P2 to meet system-specific requirements.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. This option cannot be combined with option -111 or -112.

When purchased with option -109, the 54821 supports the emerging VITA 66.5 standard and provides four optical duplex lanes to a mating VITA 66.5 backplane connector. With the installation of a serial protocol like 10 or 40 Gigabit Ethernet in the FPGA, the VITA 66.5 interface enables high-bandwidth communications between boards or chassis independent of the PCIe interface.

Options 111 and 112 provides analog signal routing through the VPX backplane. Both options replace front panel connectors for RF In, RF Out, Sample Clock/Reference Clock In and Gate/Trigger/Sync/PPS In with coax signals that pass through the backplane for connections to other boards or chassis. Option -111 is compatible with VITA 67.2. Option -112 is compatible with VITA 67.3C.

See Specifications for the OpenVPX Profile.

Navigator Design Suite

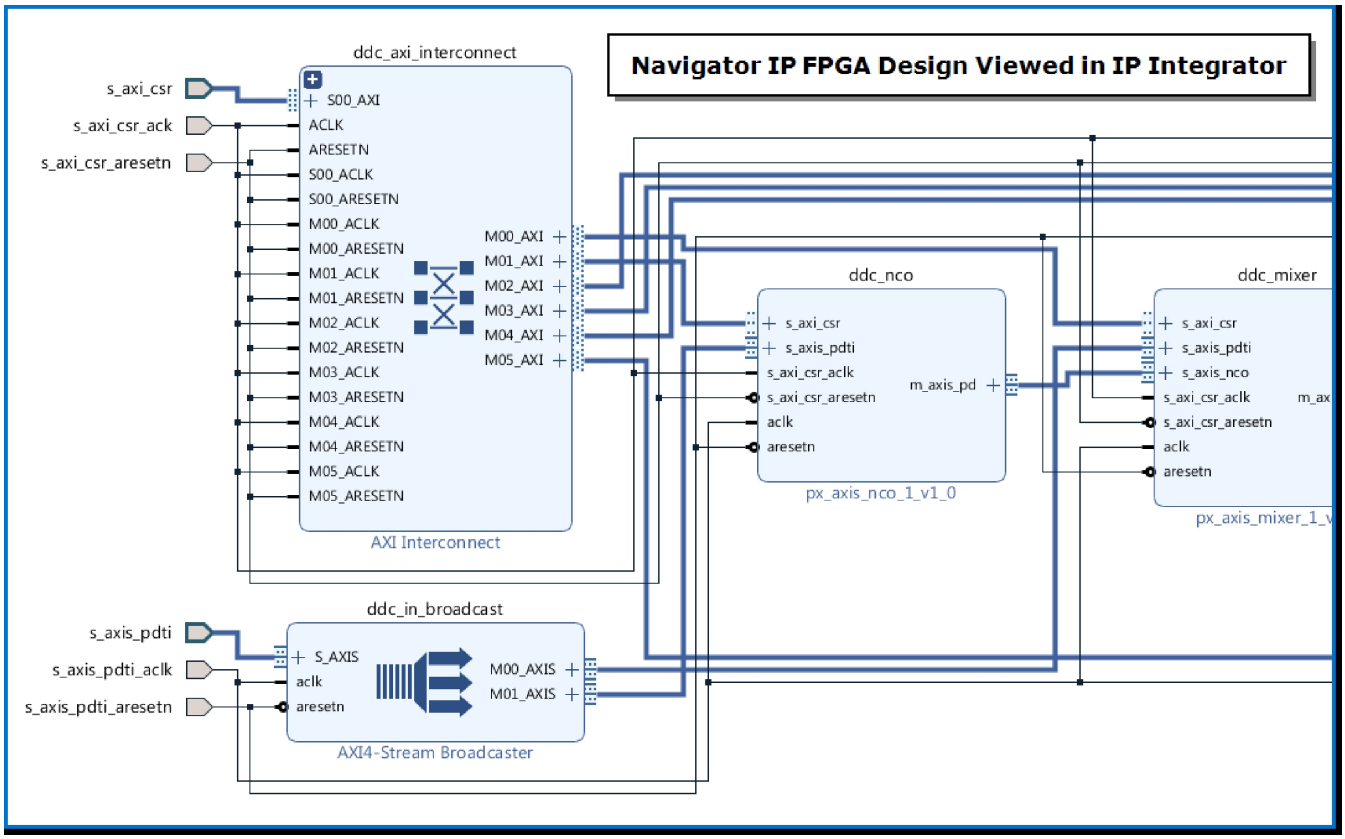
For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into Pentek's factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

NAVIGATOR Design Suite

NAVIGATOR FPGA Design Kit

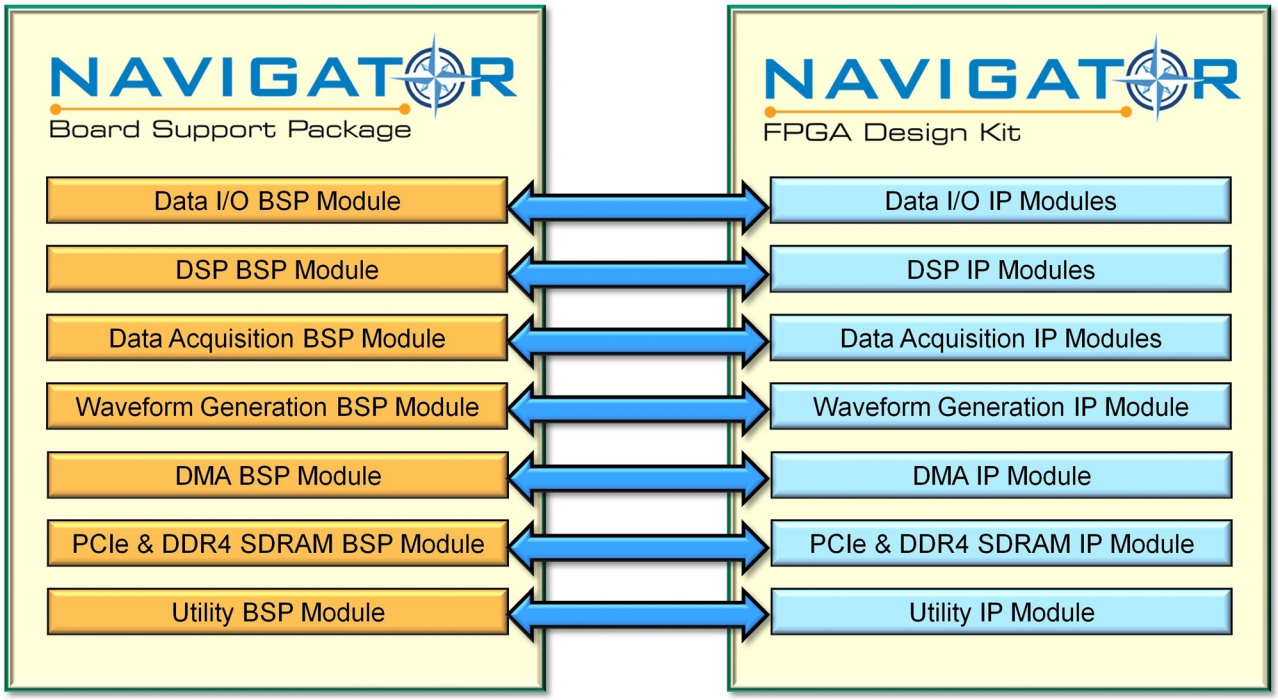
NAVIGATOR Board Support Package

The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Pentek product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Pentek design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations. Navigator FDK includes Pentek's IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.



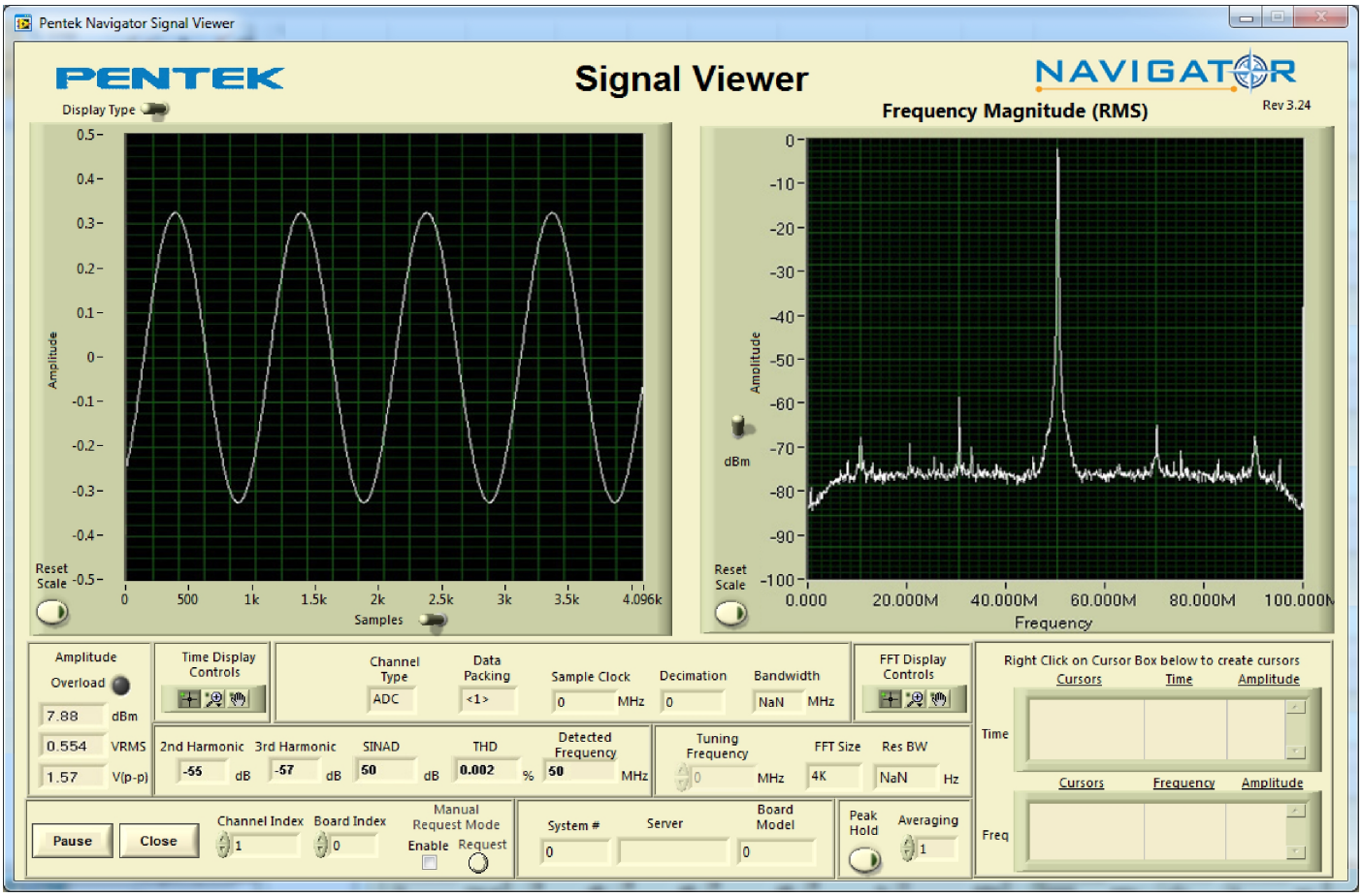
The **Navigator Board Support Package (BSP)** provides software support for Pentek boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA.

The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



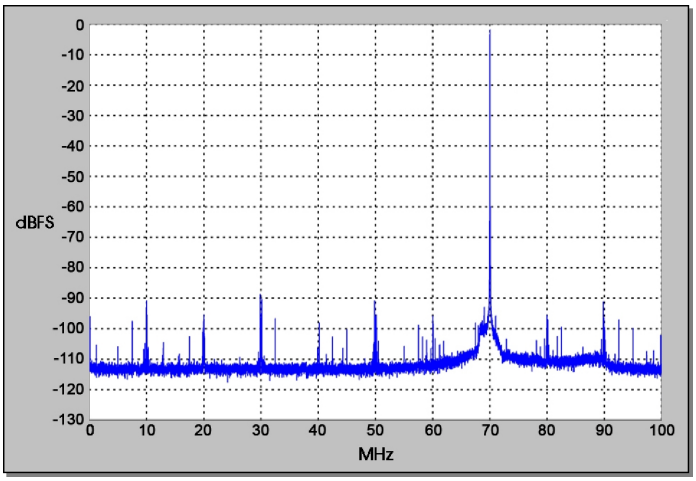
Because all Pentek boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the Signal Viewer, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Pentek hardware and Navigator BSP and start viewing analog signals immediately.



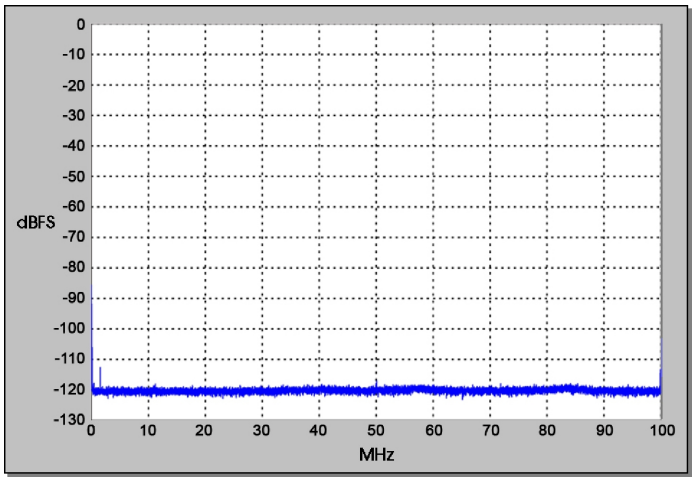
A/D Performance

Spurious Free Dynamic Range



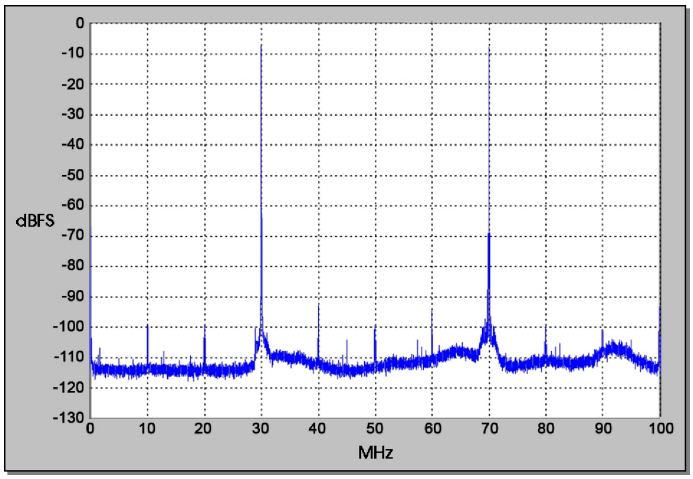
f_{in} = 70 MHz, f_s = 200 MHz, Internal Clock

Spurious Pick-up



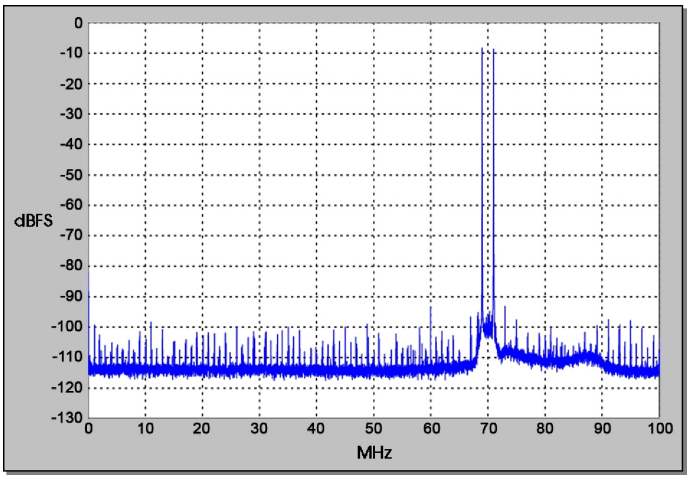
f_s = 200 MHz, Internal Clock

Two-Tone SFDR



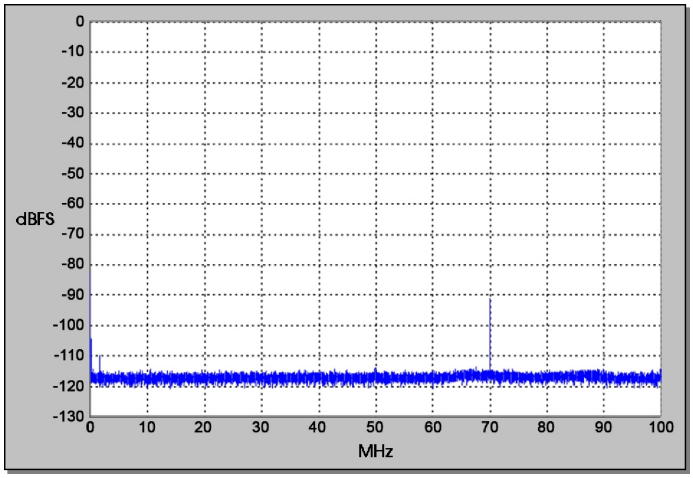
f_1 = 30 MHz, f_2 = 70 MHz, f_s = 200 MHz

Two-Tone SFDR



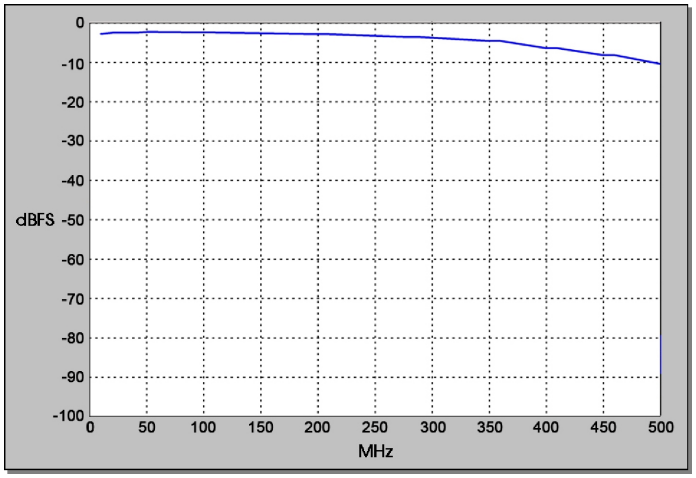
f_1 = 69 MHz, f_2 = 71 MHz, f_s = 200 MHz

Adjacent Channel Crosstalk



f_{in} Ch2 = 70 MHz, f_s = 200 MHz, Ch 1 shown

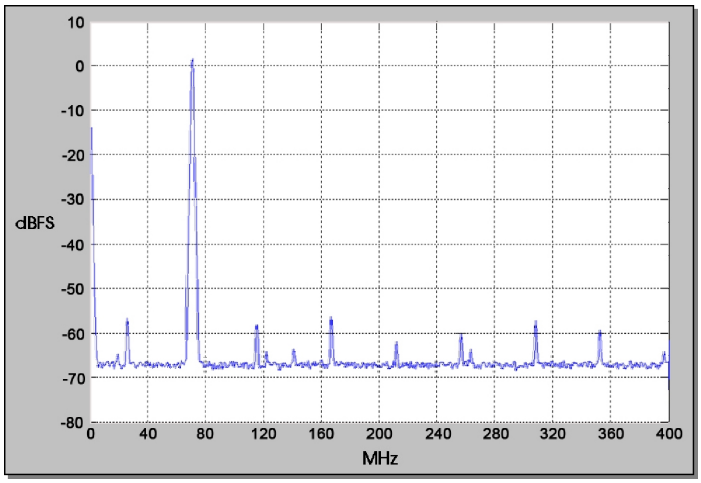
Input Frequency Response



f_s = 200 MHz, Internal Clock

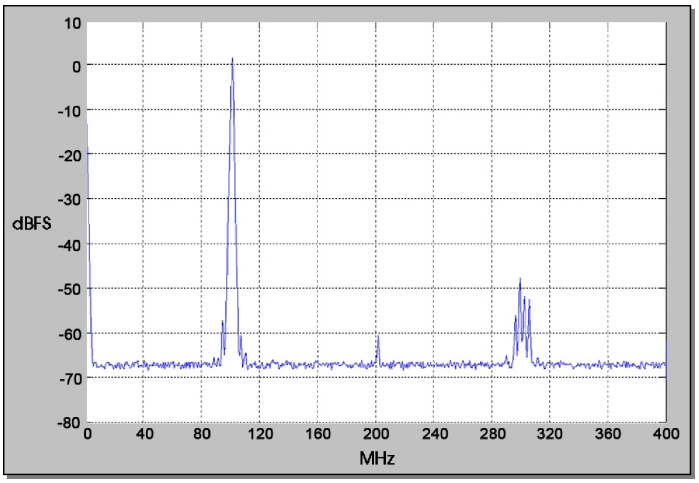
D/A Performance

Spurious Free Dynamic Range



f_{out} = 70 MHz, f_s = 800 MHz, Interpolation = 4, Internal Clock

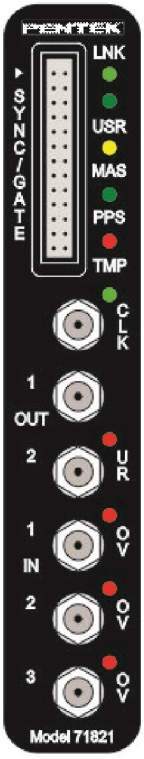
Spurious Free Dynamic Range



f_{out} = 100 MHz, f_s = 800 MHz, Interpolation = 4, Internal Clock

Front Panel Connections: Standard

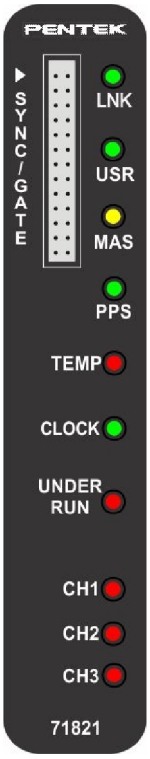
The front panel includes six SSMC coaxial connectors and a 26-pin Sync Bus connector for input/output of timing and analog signals. The front panel also includes ten LEDs.



- **Sync Bus Connector:** The 26-pin front panel connector, labeled **SYNC/GATE**, provides clock, sync, and gate input/output pins for the LVPECL Sync Bus.
- **Link LED:** The green **LNK** LED blinks when a valid link has been established over the PCIe interface.
- **User LED:** The green **USR** LED is for user applications.
- **Master LED:** The yellow **MAS** LED illuminates when this Model is the Sync Bus Master. When only a single model is used, it must be a Master.
- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the Model's PCB.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK**, for input of an external sample clock.
- **Analog Output Connectors:** Two SSMC coaxial connectors, labeled **OUT 1** and **2**: one for each DAC5688 output.
- **D/A Underrun LED:** There is one red **UR** (underrun) LED for the D/A output. This LED illuminates when the DAC5688 FIFO is out of data.
- **Analog Input Connectors:** Three SSMC coaxial connectors, labeled **IN 1**, **IN 2**, and **IN 3**: one for each ADS5485 input channel.
- **A/D Overload LEDs:** There are three red **OV** (overload) LEDs: one for each A/D input. Each LED indicates either an analog input overload in the associated ADS5485, or an A/D FIFO overrun.

Front Panel Connections: Options -111 and -112

The front panel includes a 26-pin Sync Bus connector for input/output of timing and analog signals. The front panel also includes ten LEDs. See VPX P2 for RF and clock signals.



- **Sync Bus Connector:** The 26-pin front panel connector, labeled **SYNC/GATE**, provides clock, sync, and gate input/output pins for the LVPECL Sync Bus.
- **Link LED:** The green **LNK** LED blinks when a valid link has been established over the PCIe interface.
- **User LED:** The green **USR** LED is for user applications.
- **Master LED:** The yellow **MAS** LED illuminates when this Model is the Sync Bus Master. When only a single model is used, it must be a Master.
- **PPS LED:** The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the Model's PCB.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.

- **D/A Underrun LED:** There is one red **UR** (underrun) LED for the D/A output. This LED illuminates when the DAC5688 FIFO is out of data.
- **CH LEDs:** There are three red **CH1**, **CH2** and **CH3** LEDs: one for each A/D input. Each LED indicates either an analog input overload in the associated ADS5485, or an A/D FIFO overrun.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled
Connector Type: SSMC (standard)
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters

Quantity: Three channels
Decimation Range: 2x to 32,768x in three stages of 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to fs
LO SFDR: >108 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters

Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator Core

Interpolation Range: 2x to 32,768x in three stages of 2x to 32x

Total Interpolation Range

D/A and Interpolator Core Combined: 2x to 262,144x

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled
Connector Type: SSMC (standard)
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources

On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 3, 4, 6, 8, or 16, independently for the A/D and D/A clock

External Clock

Input Type: Sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Connector Type: SSMC (standard)

Timing Bus

26-pin connector LVPECL bus includes clock-/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

Option -104: Provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O (not available with options -111 and -112)
Option -105: provides an 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols (gigabit link is 4X when combined with option -109)

VPX Options

Option -109: VITA 66.5 interface provides optical 4X duplex lanes (not available with options -111 or -112).
Option -111: VITA 67.2: RF In, RF Out and Sample Clock/Reference Clock In (these replace the front panel connectors, not available with option -109).
Option -112: VITA 67.3C: RF In, RF Out and Sample Clock/Reference Clock In (these replace the front panel connectors, not available with option -109).

Memory

Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

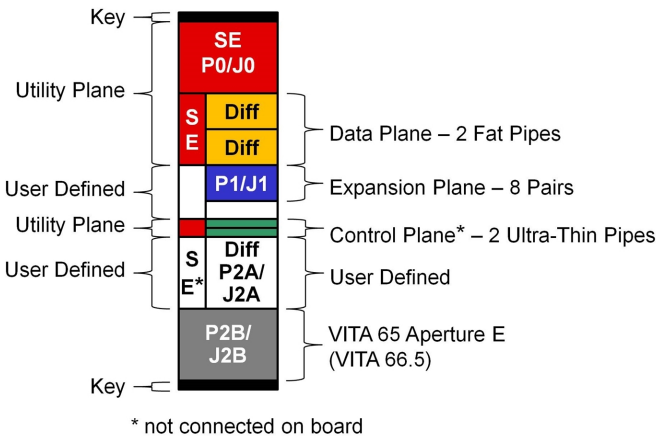
PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x8

OpenVPX Profile

The 54821 is compatible with multiple OpenVPX profiles. Profile for standard and option -109 shown below, contact Pentek for other optional profiles.

SLT3-PAY-2F2U1E-14.6.10-n.



* not connected on board

Environmental

Standard: L0 (Air-cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Option -702: L2 (Air-cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-cond.
Option -763: L3 (conduction-cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-cond.

Physical

Dimensions: 3U VPX board
Depth: 170.61 mm (6.717 in)
Height: 100 mm (3.937 in)
Weight: Approximately 15.9 oz (450 grams)

Ordering Information

Model	Description
54821	3-Channel 200 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 3U VPX

Options	Description
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through VPX P2
-105	Gigabit serial FPGA I/O through VPX P1
-109	VITA 66.5: Optical 4X duplex lanes
-111	VITA 67.2: RF In, RF Out and Sample Clock/Reference Clock In
-112	VITA 67.3C: RF In, RF Out and Sample Clock/Reference Clock In

Options	Description
-702	Air-cooled, Level 2
-741	VPX REDI compliant
-763	Conduction-cooled, Level 3
Contact Pentek for compatible option combinations and complete specifications of rugged and conduction-cooled versions. Options may change, so be sure to contact Pentek for the latest information.	

Accessory Products

Model	Description
2171	Cable Kit: SSMC to SMA
9193	System Synchronization and Distribution Amplifier

SPARK Development Systems

The Pentek SPARK® systems are fully-integrated development systems for Pentek software radio, data acquisition, and I/O boards. They were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

The following SPARK systems are available for Pentek's Cobalt®, Onyx®, and Jade® boards: PCIe (Model 8266), 3U OpenVPX (Model 8267) and 6U OpenVPX (Model 8264). For Flexor boards, SPARK systems are available in PCIe (Model 8266) and 3U VPX (Model 8267).

Pricing and Availability

To learn more about our products or to discuss your specific application please contact your local representative or Pentek directly:

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