



**PENTEK**  
SOFTWARE &  
FPGA TOOLS

# SOFTWARE & FPGA TOOLS

## MODEL

## DESCRIPTION

[4811, 4814, 4815](#)

Navigator™ Design Suite

[4953](#)

Pentek GateFlow® FPGA Design Kit

[4994A](#)

Pentek ReadyFlow BSPs for Linux

[4995A](#)

Pentek ReadyFlow BSPs for Windows®

[4996/4996A](#)

Pentek VxWorks BSPs and Drivers

[VxWorks](#)

Wind River Workbench/VxWorks for PowerPC

—

Pentek SystemFlow® Recording Software for Talon Recorders

[Customer Information](#)

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Last updated: April 2018

### General Information

Pentek's Navigator Design Suite includes the Navigator FDK (FPGA Design Kit) for integrating custom IP into the Pentek factory-shipped design and the Navigator BSP (Board Support Package) for creating host applications. The Navigator Design Suite takes a new approach to solving FPGA IP and control software connectivity.

Most modern FPGA-processing applications require development of specialized FPGA IP to run on the hardware, *and* software to control the FPGA hardware from a host computer.

Even when "turnkey" solutions are delivered with complete FPGA IP and software libraries, as developers add their own custom-processing IP, new software needs to be created to control the custom IP functions.

Problems often arise when the IP and software development tools treat application development as two separate tasks. Changes to FPGA IP and control software can quickly get out of sync, complicating new application development or even breaking the formally functioning turnkey components.

The Navigator Design Suite was designed from the ground up to work with Pentek's Jade™ architecture and provide a better solution to the complex task of IP and software creation.



### Navigator FDK (FPGA Design Kit)

As FPGAs become larger and IP more complex, the need for IP design tools to manage this growing complexity has never been greater.

The Xilinx Vivado Design Suite includes IP Integrator, the industry's first plug-and-play IP integration design environment. Built around a graphical block diagram interface, IP Integrator allows IP developers to leverage existing IP by importing it into their block diagram design. Pentek's Navigator FPGA Design Kit (FDK), was designed with this exact purpose.

Each Navigator FDK provides the complete IP for a specific Jade data acquisition and processing board. When the design is opened in Vivado's IP Integrator, the developer can access every component of the Pentek design, replacing or modifying blocks as needed for the application. All blocks use industry standard AXI4 interfaces providing a well-defined format for custom IP to connect to the rest of the design. Each Navigator/Jade design includes User Blocks in the data-flow path, ideal for inserting custom processing IP.

The Navigator FDK includes complete documentation, test benches and full VHDL source for developers who desire complete access to the IP. In addition to the IP specific to the supported Jade board, Navigator also includes processing blocks for some of the most commonly used algorithms. ▶



As a Certified Member of Xilinx's Alliance program, Pentek has passed a comprehensive 320-point review of its technical, business, quality, and support processes and has committed engineers who completed the same rigorous training used by Xilinx Field Application Engineers worldwide.

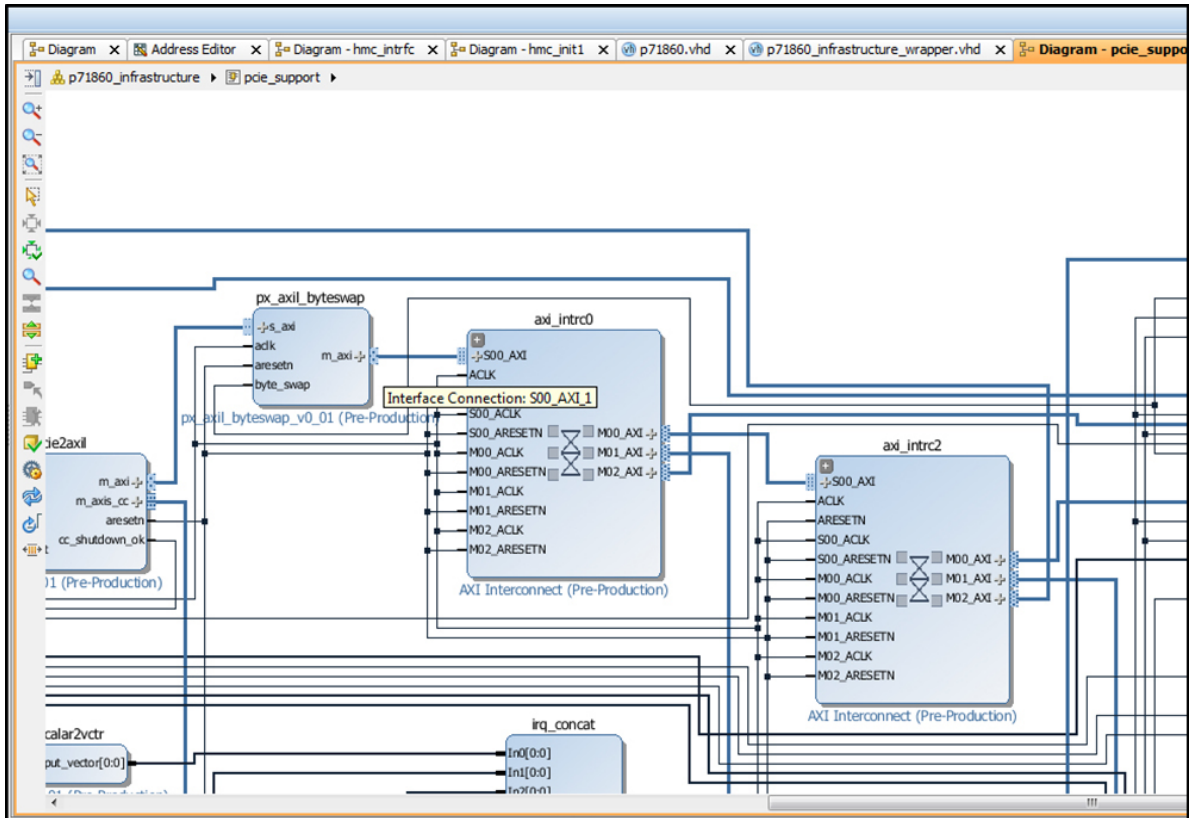
Pentek continues to demonstrate years of expertise with Xilinx devices and implementation techniques that consistently deliver high-quality products and services utilizing the Xilinx programmable platforms.



The Model 78861 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today.

Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

This XMC board is also available in other formats such as 3U and 6U VPX, PCIe, 3U and 6U cPCI, and AMC.



As shown in the above screen shot, Navigator IP blocks work directly in Xilinx Vivado.

The screenshot shows the Navigator IP block repository in Xilinx Vivado. A search bar is visible at the top. Below it, a table lists various IP blocks available for selection.

Name	AXI4	Status	License	VLNV
User Repository (e:/px_ip)				
PentekIP				
openhmc_ctr_v0_01	AXI4-Stream	Pre-Production Included	pentek.com...	
p_axil_csr32_v0_1	AXI4	Pre-Production Included	pentek.com...	
px_ads5485intrfc_v0_01	AXI4, AXI4-Stream	Pre-Production Included	pentek.com...	
px_axil2cdc_v0_01	AXI4	Pre-Production Included	pentek.com...	
px_axil2hmc_v0_01	AXI4, AXI4-Stream	Pre-Production Included	pentek.com...	
px_axil_addr_sub_v0_01	AXI4	Pre-Production Included	pentek.com...	
px_axil_bram_ctr_v0_01	AXI4	Pre-Production Included	pentek.com...	
px_axil_byteswap_v0_01	AXI4	Pre-Production Included	pentek.com...	
px_axil_csr_v0_01	AXI4	Pre-Production Included	pentek.com...	
px_axil_j2c_mstr_v0_01	AXI4	Pre-Production Included	pentek.com...	
px_axil_nativefifo_ctr_v0_01	AXI4	Pre-Production Included	pentek.com...	
px_axis_pdt2ppkt_1_v0_01	AXI4, AXI4-Stream	Pre-Production Included	pentek.com...	
px_axis_pdti_adv_v0_01	AXI4, AXI4-Stream	Pre-Production Included	pentek.com...	
px_axis_pdti_mrg_v0_01	AXI4-Stream	Pre-Production Included	pentek.com...	
px_axis_pdti_split_v0_01	AXI4-Stream	Pre-Production Included	pentek.com...	
px_axis_pwr_meter_v0_01	AXI4, AXI4-Stream	Pre-Production Included	pentek.com...	
px_axis_round_v0_01	AXI4-Stream	Pre-Production Included	pentek.com...	
px_axis_thresh_det_v0_01	AXI4, AXI4-Stream	Pre-Production Included	pentek.com...	
px_axis_tieoff_v0_01	AXI4-Stream	Pre-Production Included	pentek.com...	
px_axis_traffic_meter_v0_01	AXI4, AXI4-Stream	Pre-Production Included	pentek.com...	
px_axispdti_4mux_v0_01	AXI4, AXI4-Stream	Pre-Production Included	pentek.com...	
px_axispdti_8mux_v0_01	AXI4, AXI4-Stream	Pre-Production Included	pentek.com...	
px_brd_info_regs_v0_01	AXI4	Pre-Production Included	pentek.com...	
px_cdc_clk_intrfc_v0_01	AXI4	Pre-Production Included	pentek.com...	
px_consthex32_v0_01		Pre-Production Included	pentek.com...	
px_dma_hmc2pcie_v0_01	AXI4, AXI4-Stream	Pre-Production Included	pentek.com...	
px_dma_pcie2hmc_v0_01	AXI4, AXI4-Stream	Pre-Production Included	pentek.com...	
px_dma_ppkt2hmc_v0_01	AXI4, AXI4-Stream	Pre-Production Included	pentek.com...	
px_dma_ppkt2pcie_v0_01	AXI4, AXI4-Stream	Pre-Production Included	pentek.com...	
px_oate_express_v0_01	AXI4, AXI4-Stream	Pre-Production Included	pentek.com...	

Details: Select an IP to see details

This screen shot shows Navigator IP blocks which are selectable from a pull-down menu.

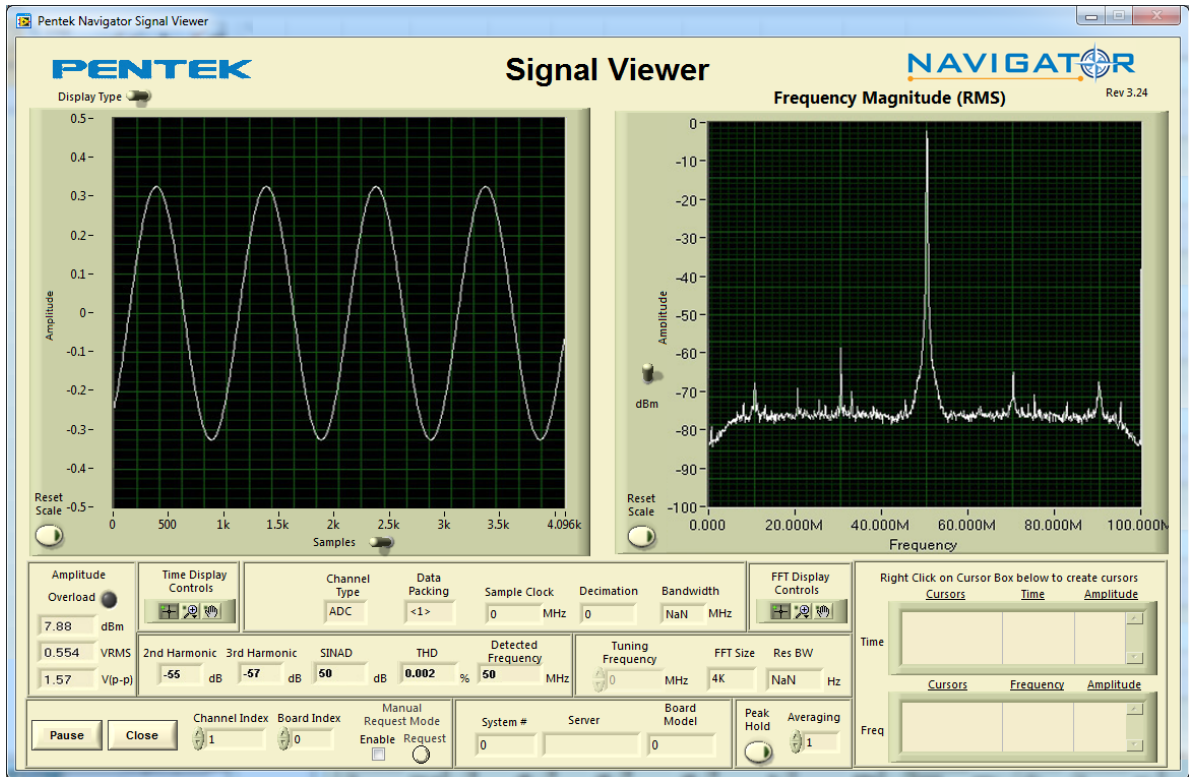
Navigator BSP (Board Support Package)

The companion product to the Navigator FDK is the Pentek Navigator Board Support Package (BSP). While Navigator FDK provides a streamlined path for creating or modifying new IP for the Pentek hardware, the Navigator BSP enables complete operational control of the hardware and all IP functions in the FPGA.

Similar to the FDK, the BSP allows software developers to work at a higher level, abstracting many of the details of the hardware through an intuitive API. The API allows developers to focus on the task of creating the application by letting the API, the hardware and IP-control libraries below it to handle many of the board-specific functions. Developers who want full access to the entire BSP library, enjoy complete C-language source code as well as full documentation.

New applications can be developed on their own or by building on one of the included example programs. All Jade boards are shipped with a full suite of built-in functions allowing operation without the need for any custom IP development. Many users find these functions ideal for addressing their application requirements.

The Navigator BSP includes the Signal Analyzer, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Analyzer users can install the Pentek hardware and Navigator BSP and start viewing analog signals immediately. ➤



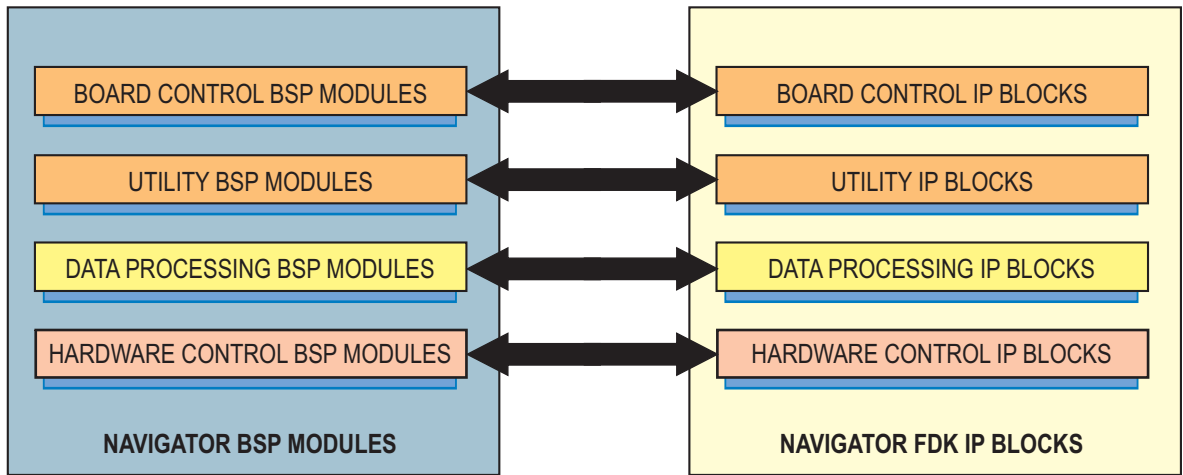
Navigator BSP Signal Analyzer

**Optimize BSP and IP Development**

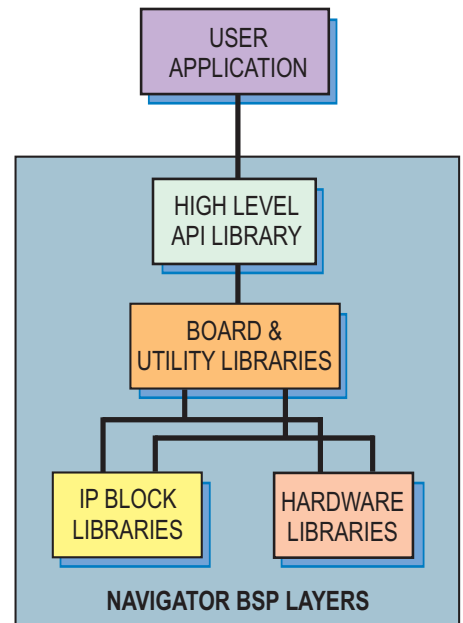
For users who need to develop applications that include custom IP, the combination and compatibility of Navigator FDK and Navigator BSP streamline development.

When new IP is introduced into the design, it has the potential of changing how the hardware looks to the host, possibly breaking the software. Navigator FDK and BSP were designed together to closely match the FPGA IP blocks and the BSP functions that control them. As developers modify IP they can easily find the corresponding BSP functions and modify them in parallel.

Navigator FDK uses AXI4 for all IP block interfaces. When developers create their own IP blocks using AXI4, they are immediately compatible with the Pentek-supplied IP. Following the Navigator BSP style guide, users can similarly create BSP modules for compatibility with the Navigator BSP library.



*Optimized BSP and IP Development*



*Optimized BSP and IP Development*

**Ordering Information**

Model	Description
4811	Navigator FDK (FPGA Design Kit)
4814	Navigator BSP (Board Support Package) for Linux
4815	Navigator BSP (Board Support Package) for Windows



**GateFlow®** is Pentek's family of extendable FPGA products. The GateFlow product line includes the *GateFlow FPGA Design Kit* to ease custom algorithm development and the *GateFlow Factory-installed IP Cores* in Pentek FPGA board products.

The Pentek Model 4953 GateFlow FPGA Design Kit provides the user with design information, software files and utilities for extending FPGA functions in these products.

Users can implement a variety of custom preprocessing functions such as convolution, framing, pattern recognition, decompression, FFT, delay, decoding, time stamping, averaging, summation and many more.

### Using the FPGA Design Kit

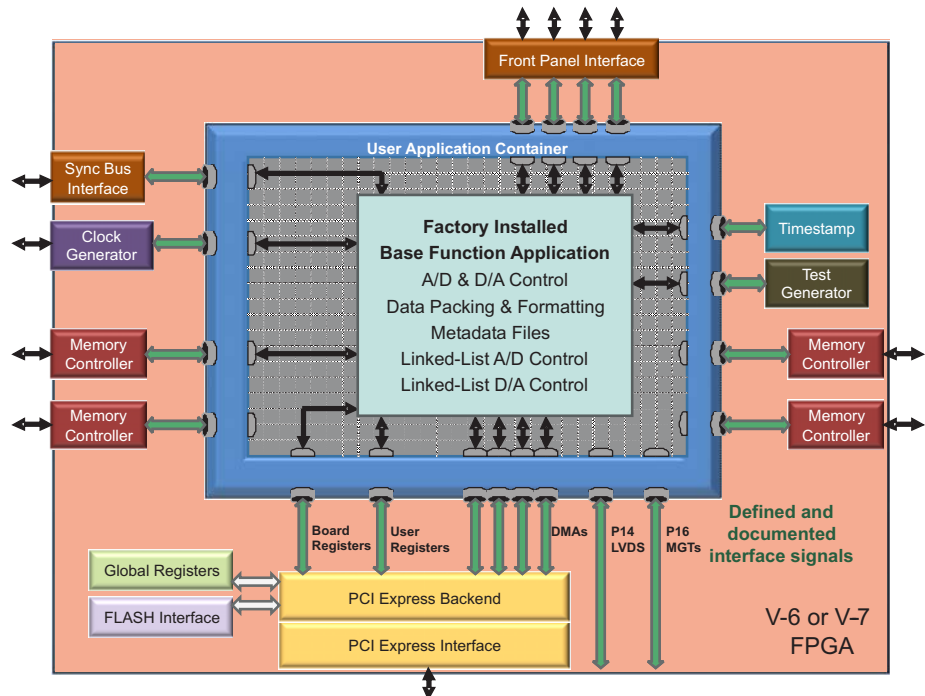
The **GateFlow** FPGA Design Kit allows the user to modify, replace and extend the standard factory-installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt, Onyx and Flexor architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower level details of the hardware.

### The User Application Container

Shown below is the FPGA block diagram of a typical Cobalt, Onyx or Flexor module. The User Application Container holds a collection of different factory-installed IP modules connected to the various interfaces through the standard ports that surround the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow Design Kit provides a complete Xilinx ISE Foundation or Vivado project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each module provides an example of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.



FPGAs in Pentek Products

The chart below shows the Xilinx FPGA families used in the three Pentek families of board-level products. These products use some FPGA resources to implement standard factory functions as well as installed IP cores.

The chart shows the approximate percentage of unused system slices and RAM available to the user for extending the FPGA to include custom algorithms for the user's application.



Available FPGA Resources for Pentek Boards

			Xilinx Virtex-6			Xilinx Virtex-7			Xilinx Kintex UltraScale					
			LX130T	LX240T	SX315T	VX330T	VX690T	KU035	KU060	KU115				
Logic Cells			128,000	241,152	314,880	326,400	693,120	444,340	725,550	1,451,100				
CLB Slices			20,000	37,680	49,200	51,000	108,300	203,120	331,680	663,360				
CLB Flip-Flops			160,000	301,440	393,600	408,000	866,400	406,255	663,360	1,326,720				
Max. Block RAM			9,504 kb	14,976 kb	25,344 kb	27,000 kb	52,920 kb	5.9 Mb	9.3 Mb	18.3 Mb				
DSP 48E Blocks			480	768	1,344	1120	3,600	1,700	2,760	5,520				
PCI Express Support			Gen 2, x8	Gen 2, x8	Gen 2, x8	Gen 3, x8	Gen 3, x8	Gen 3, x8	Gen 3, x8	Gen 3, x8				
Pentek Model	Board Type	No. of FPGAs	% Available to User						% Available to User					
			Slices		RAM		Slices		RAM		Slices		RAM	
71620*	XMC	1	68%	75%	83%	82%	87%	90%	-	-	-	-	-	-
71621*	XMC	1	-	-	66%	63%	74%	78%	-	-	-	-	-	-
71624*	XMC	1	-	-	-	-	N/A	N/A	-	-	-	-	-	-
71630*	XMC	1	55%	64%	76%	77%	81%	86%	-	-	-	-	-	-
71640*	XMC	1	8%	64%	46%	77%	59%	86%	-	-	-	-	-	-
71641*	XMC	1	-	-	-	-	N/A	N/A	-	-	-	-	-	-
71650*	XMC	1	66%	74%	82%	84%	86%	90%	-	-	-	-	-	-
71651*	XMC	1	-	-	47%	65%	58%	79%	-	-	-	-	-	-
71660*	XMC	1	69%	75%	76%	85%	88%	92%	-	-	-	-	-	-
71661*	XMC	1	-	-	43%	67%	73%	81%	-	-	-	-	-	-
71662*	XMC	1	-	-	N/A	N/A	48%	62%	-	-	-	-	-	-
71663*	XMC	1	-	-	-	-	N/A	N/A	-	-	-	-	-	-
71670*	XMC	1	24%	46%	58%	65%	68%	80%	-	-	-	-	-	-
71671*	XMC	1	-	-	58%	65%	68%	80%	-	-	-	-	-	-
71690*	XMC	1	80%	87%	89%	91%	91%	95%	-	-	-	-	-	-
71720**	XMC	1	-	-	-	-	-	-	52%	80%	77%	90%	-	-
71721**	XMC	1	-	-	-	-	-	-	44%	69%	71%	16%	-	-
71730**	XMC	1	-	-	-	-	-	-	52%	80%	77%	90%	-	-
71741**	XMC	1	-	-	-	-	-	-	40%	77%	69%	88%	-	-
71751**	XMC	1	-	-	-	-	-	-	48%	75%	75%	87%	-	-
71760**	XMC	1	-	-	-	-	-	-	76%	83%	78%	91%	-	-
71761**	XMC	1	-	-	-	-	-	-	43%	73%	70%	86%	-	-
71131***	XMC	1	-	-	-	-	-	-	-	-	-	-	TBD	TBD
71132***	XMC	1	-	-	-	-	-	-	-	-	-	-	TBD	TBD
71141***	XMC	1	-	-	-	-	-	-	-	-	-	-	TBD	TBD
71821***	XMC	1	-	-	-	-	-	-	-	-	-	-	TBD	TBD
71841***	XMC	1	-	-	-	-	-	-	-	-	-	-	TBD	TBD
71851***	XMC	1	-	-	-	-	-	-	-	-	-	-	TBD	TBD
71861***	XMC	1	-	-	-	-	-	-	-	-	-	-	TBD	TBD
71862***	XMC	1	-	-	-	-	-	-	-	-	-	-	TBD	TBD

\*Cobalt form factors: 716xx = XMC; 726xx = 6U CPCI; 736xx = 3U cPCI; 746xx = 6U CPCI (Dual XMC); 786xx = x8 PCIe; 536xx = 3U VPX - Format 1; 526xx = 3U VPX - Format 2; 566xx = AMC; 576xx = 6U VPX; 586xx = 6U VPX (Dual XMC)  
 \*\*Onyx form factors: 717xx = XMC; 727xx = 6U CPCI; 737xx = 3U cPCI; 747xx = 6U CPCI (Dual XMC); 787xx = x8 PCIe; 537xx = 3U VPX - Format 1; 527xx = 3U VPX - Format 2; 567xx = AMC; 577xx = 6U VPX; 587xx = 6U VPX (Dual XMC)  
 \*\*\*Kintex form factors: 718xx = XMC; 728xx = 6U CPCI; 737xx = 3U cPCI; 748xx = 6U CPCI (Dual XMC); 788xx = x8 PCIe; 538xx = 3U VPX - Format 1; 528xx = 3U VPX - Format 2; 568xx = AMC; 578xx = 6U VPX; 588xx = 6U VPX (Dual XMC)  
 Some Kintex Ultra Scale products use 1 in place of 8 - TBD: To Be Determined - N/A: Not Available



## General Information

Users of high-performance data acquisition and signal processing boards often find themselves frustrated by the fact that when their new devices are delivered, they are unable to put them to immediate use.

Because these boards are largely software controlled and offer a flexible range of functionality, a certain amount of programming is generally necessary to put the new cards through their paces. Then, if something does not go as planned, there is no way of knowing for sure whether the problem lies with the new code, or with the hardware itself.

To address this issue, Pentek has developed the **ReadyFlow**® BSPs (Board Support Packages) for all its board-level products. These packages:

- Provide a path for quick start-up through application completion
- Allow programming at high, intermediate and low levels to meet various needs
- Are illustrated with numerous examples
- Include complete documentation and definitions of all functions
- Include library and example source code

## What's Included in the Package

In general, functions appropriate to the board-level product, such as:

- A "How to" section
  - Build object libraries
  - Compile and link application programs
- C-callable functions
  - Initialization and test
  - Data movement and communications
  - Backplane I/O
  - Mezzanine peripheral I/O
  - Control of board resources
- Utilities
  - Flash memory program loaders

The package contains C-language examples that can be used to demonstrate the capabilities of Pentek products. The examples included provide the answers to

most of the questions that occur with first-time users of Pentek products.

These programming examples will also help you get an immediate start on writing your own application without having to reinvent the wheel. They provide sample code that is known to work, giving you, the new user, a means of verifying that your board set is operational.

ReadyFlow Board Support Packages are designed to reduce development time not only during the initial stages, but any time new hardware is added to the system. All packages are built with a consistent style and function-naming convention. Similar parameters on different boards have similar function calls, thereby allowing immediate familiarity with new hardware as it's added further shortening the learning curve.

## Command Line Interface

The Command Line Interface provides access to precompiled executable examples that operate the hardware right out of the box, without the need to write any code.

Board-specific hardware operating arguments can be entered in the command line to control the following parameters: number of channels to enable, sample clock frequency, data transfer size, data rate divider, interpolation factor, reference clock frequency, reference clock source, number of iterations to run the program, etc.

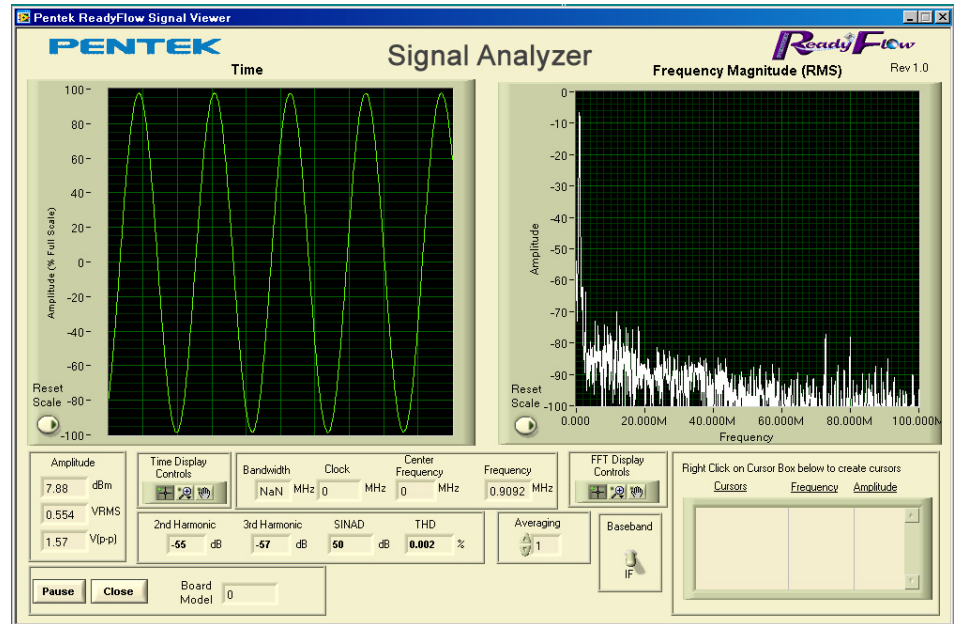
Below is an example command line for D/A capable hardware that enables the channel one output, transfers 32,768 data bytes, executes 100,000 times, divides the data rate by 2, and interpolates the data by 4:

```
C:> dacmode -chan 1 -xfersize 32768
      -loop 100000 -ratediv 2
      -interpolate 4
```

The Command Line Interface can be used to call an example application from within a larger user application to control the hardware, and parameter arguments are passed to the application for execution. Functions that control data acquisition, automatically save captured data to a pre-named host file or are routed to the Signal Analyzer example function for display. ►



For the latest list of boards supported with ReadyFlow, visit our website at:  
[www.pentek.com/readyflow](http://www.pentek.com/readyflow)



### Signal Analyzer\*

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals

### Example, Model 71620

As an example of XMC module support, the BSP for the Cobalt® Model 71620 Transceiver with three 200 MHz A/Ds, DUC (Digital Upconverter), and two 800 MHz D/As includes data structures and routines to support the following:

- PCIe Bus interface and DMA controller
- Board control registers
- Timing bus control and clock selection
- Triggering, gate enable and polarity
- Data input device management for the 200 MHz A/D
- Data output device management for the DUC and the 800 MHz D/A
- Built-in A/D Data Acquisition IP Modules
- Built-in D/A Waveform Playback IP Modules
- Built-in test waveform generator
- Interrupt generation and handling
- FPGA configuration
- Test modes and hardware revision codes
- Hardware voltage and temperature monitor

## Ordering Information

### Model Description

4994A ReadyFlow - Board Support Package for Linux

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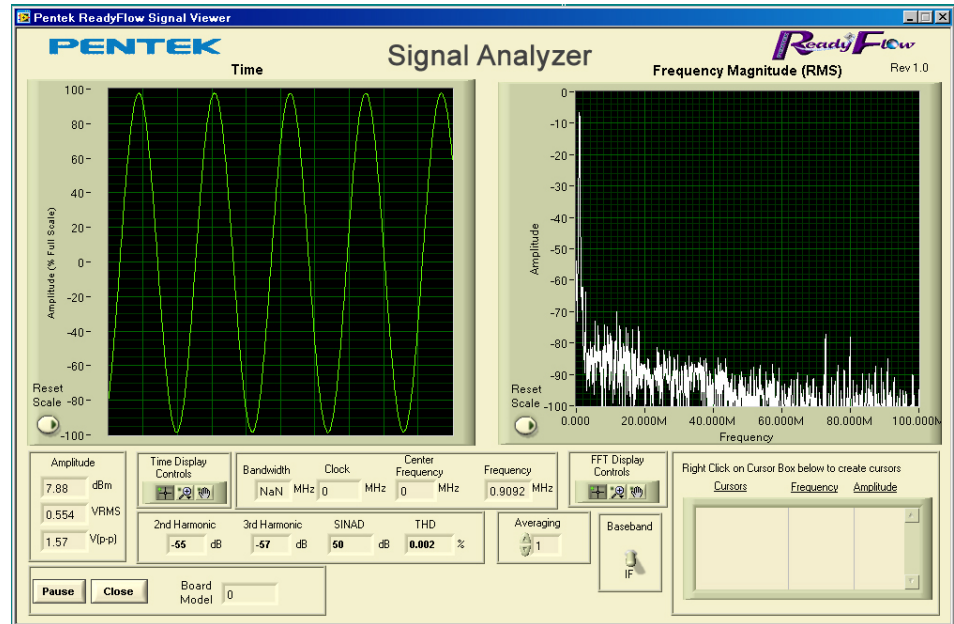
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For the latest list of boards supported with ReadyFlow, visit our website at:  
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### Ordering Information

#### Model Description

4995A ReadyFlow - Board Support Package for Windows


 WIND RIVER  
PARTNER

### Ordering Information

Model	Description
4996/4996A	Pentek VxWorks BSPs and Hardware Drivers

Contact Pentek for availability

The Models 4996/4996A VxWorks BSPs provide software developers with a complete library of hardware initialization, control and application functions for Pentek PowerPC®/Power Architecture® processor baseboards, VME/VXS, PMC/XMC, VIM, and cPCI boards and modules. Used in conjunction with Wind River's **Workbench**® software development environment, they speed application development by providing a high-level API for accessing all of the processor board's memory and communication resources, and control of the board's I/O interfaces and I/O modules.

Processor specific functions found in the baseboard BSPs include: cache, DMA, SDRAM, interrupt, serial port, and timer control. Some general board functions include: reading and writing to mezzanine board FIFOs, VME/VXS, PMC/XMC, cPCI, and VIM I/O control, interprocessor commu-

nication, programming DMA reads and writes, programming interrupts, using mailboxes, managing RS-232 and ethernet interfaces, and control of optional Fibre Channel interfaces.

The VxWorks BSPs are designed to reduce development time not only during the initial stages of software development, but any time new I/O hardware is added to the system. **Hardware Drivers**, each designed to control the specific hardware features of the I/O interface being used, are built with a consistent style and function naming convention. Similar parameters on different I/O modules have similar driver calls, thereby allowing immediate familiarity with new I/O hardware as it's added. This can greatly shorten the application development learning curve when a system is modified or expanded.

### Ordering Information

Contact Wind River Systems at:  
[www.windriver.com](http://www.windriver.com)

Wind River's **Workbench** development platform has dramatically improved embedded developers' "time-to-productivity". A component of Workbench, Workbench Tools, comprises a comprehensive suite of core and optional cross-development tools and utilities. The other integrated components of Workbench consist of the VxWorks run-time system, a high-performance scalable real-time operating system that executes on the target processor and a full range of communications options for the target connection to the host. Workbench Tools provides a

highly visual and automated environment that accelerates the development of even the most complex VxWorks-based applications.

At the heart of the VxWorks run-time system is the highly efficient Wind microkernel which supports a full range of real-time features. These include fast multitasking, interrupt support, and both preemptive and round-robin scheduling. The microkernel design minimizes system overhead and enables fast, deterministic response to external events.



## Features

- Complete turnkey recording and/or playback system software for Talon Recording Systems
- Software API for controlling data acquisition and recorder functions
- Graphical user interface
- Windows or Linux host
- One-year support included

## General Information

The Pentek SystemFlow Recording Software provides a rich set of function libraries and tools for controlling and building Pentek's real-time recording and data acquisition systems. These libraries ensure a consistent look and feel for developers across system families.

SystemFlow software allows developers to configure and customize system interfaces and behavior. It includes API functions not only for the real-time data acquisition and playback functions, but also for the user-control software running on the host PC including the GUI. These API functions allow developers to either modify the sample code to meet their needs or use it as a reference for custom software development.

## API Library Components

SystemFlow is based on a flexible client/server architecture. The host client application runs on a Windows or Linux platform and communicates with the server target application via a standard socket connection. In this way, server real-time recording and/or playback operations can be controlled from a local or remote host client.

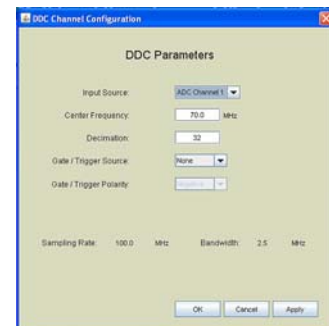
All servers use PC hardware running under Windows. The server application includes scheduling, task management, full control of data from Pentek software radio hardware, and drivers for communication with the hard disk arrays.

## SystemFlow Recorder Interface

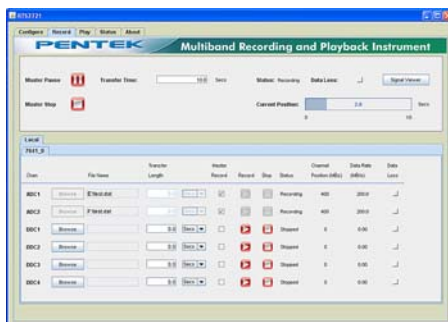
The SystemFlow GUI provides the user with a control interface for recording data. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or recorded signals on disk.

## Hardware Configuration Interface

The SystemFlow configuration screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, provides entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.



Hardware Configuration Interface

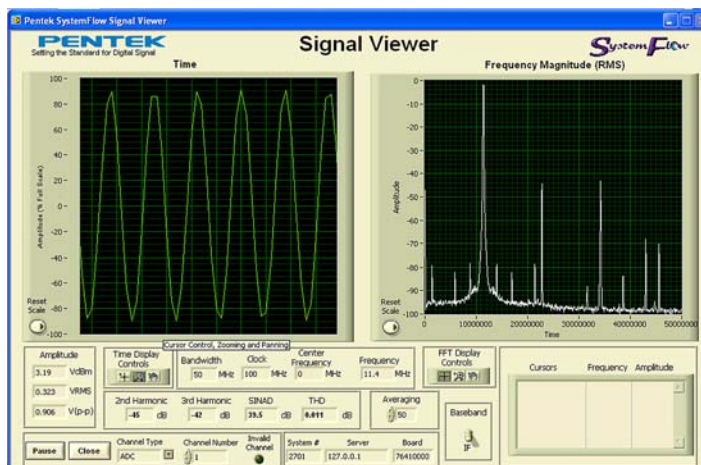


Recorder Interface

## SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.



Signal Viewer

More information on [pentek.com](http://pentek.com)

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[Return Material Authorization Form](#)

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Carefully package the product in its original packaging, if it is still available, and ship it to Pentek prepaid (if within the US) or free domicile DDP (if outside the US). Pentek shall not be responsible for loss or damage in shipment to Pentek, so you are strongly encouraged to insure the shipment for its full replacement value.

When the work is completed, we will return the product to you along with a statement of work performed.

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