New RF FPGA solutions transform EW platforms

Story

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RODGER HOSKING

Pentek, now part of Mercury

Maintaining a tactical advantage in EW (electronic warfare) has become one of the highest priorities for defense organizations. Ongoing development of innovative strategies and evolution of technologies are necessary to counter new threats and to exploit new targets.

Recent advances in silicon technology aggregate many essential elements required in electronic warfare (EW) systems within a single device. These highly integrated components not only simplify traditional EW design architectures, but also add critical performance metrics. Because they can reduce size, weight, power, and cost (SWaP-C), they also open new markets and application spaces that were previously impractical.

Presented with diverse and challenging requirements and tight schedules, EW system designers must take advantage of any new resources or design strategies suitable to the tasks at hand.

EW operational challenges

EW exploits the entire electromagnetic spectrum to gain advantage over the enemy with an incredibly diverse range of deployed platforms for land, air, sea, underwater, and space environments. EW is divided into three application areas: electronic attack (EA) for classic offensive objectives to disrupt, deny, degrade, destroy or deceive; electronic protection (EP), which seeks to thwart the effectiveness of EA; and electronic support (ES), which harvests the extensive wealth of signal information of all types to improve decision-making and strategies. Despite the many differences across these platforms, they share many common needs, so that a new effective technology implemented on one platform is often quickly adapted by others.

Modern EW systems for radar, communications, telemetry, and interception now increasingly rely upon phased-array antennas to steer receive and transmit signal beam patterns. These antennas are usually linear or two-dimensional planar arrays often containing dozens of elements, each requiring separate signal processing for precisely shifting the phase to attain the desired directionality. They can be installed on a hull surface and quickly adapt to threats and targets without the bulky mechanical structures required for a directional dish. Although ideally suited for airborne and UAV [unmanned aerial vehicle] radars where size is critical, larger phased arrays are also extremely effective for precision ground- and maritime-based radars as well, especially for fire-control systems and countermeasures.

These larger phased-array systems pose several new challenges for the traditional EW system architecture where the antenna array is mounted in a location best suited to capture signals (perhaps on an antenna mast) and connected with radio frequency (RF) cables down to an equipment bay through dozens of long RF cables for each of the elements. Maintaining beam-steering integrity requires preserving precise and stable phase matching between those cables despite temperature fluctuations, physical movement, aging, and maintenance issues. To make matters worse, analog signals flowing from remote antennas or sensors suffer signal degradation from cable losses and susceptibility to interference from powerful antenna transmit signals, interchannel crosstalk, and power-generation equipment.

Many EA and EP systems are dedicated to fire-control and countermeasures, in which a signal is received and a counter response is computed and then delivered, all as quickly as possible. This overall latency often defines the limiting factor in the effectiveness of such systems. Unfortunately, the latest data-converter devices (both analog-to-digital [ADC] and digital-to-analog [DAC]) with the highest sampling rates now favor gigabit serial JESD204 interfaces to achieve high data I/O transfer rates. Even though they achieve high instantaneous bandwidths, the interfaces on these devices rule out use in low-latency EW applications.

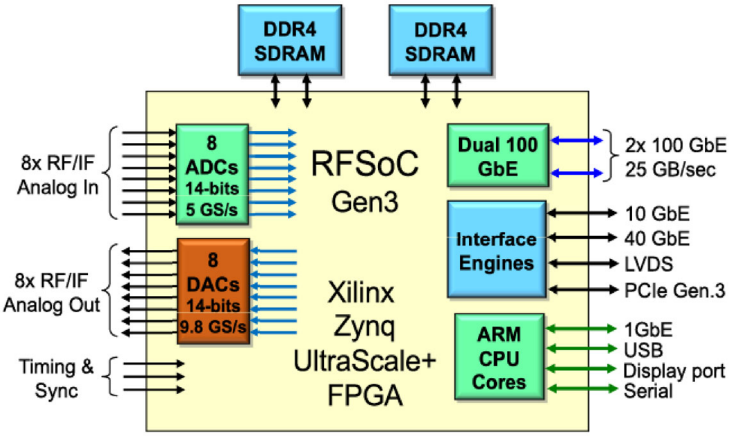
Relentless increases in RF signal complexity are driven by the need to conserve precious bandwidth in the overcrowded frequency spectrum. Here, sophisticated radar pulse waveforms are developed to extract more information from targets despite noise, jamming and other countermeasures; signals are also heavily encrypted for enhanced security against interception and eavesdropping. For EA and EP systems, low-latency, real-time digital signal processing (DSP) is essential to overcome these obstacles to compute an immediate and appropriate response with minimal delay. This function is usually accomplished with field-programmable gate arrays (FPGAs), although some of the higher-complexity tasks can require GPUs or AI engines.

Compounding the data converter and signal processing issues above, phased-array systems magnify these challenges because each of the numerous elements now requires its own dedicated ADC, DAC, and DSP function. This impacts size, weight, and power (SWaP) metrics as well as cost, greatly depending on the implementation.

New FPGA RF technology for EW systems

Xilinx offers two families of solutions to the many challenges above by combining critical EW functions within a single device. The first family of such technology was the RFSoC (RF system-on-chip).

Introduced in 2017, RFSoC uses the Xilinx UltraScale+ FPGA Zynq architecture based on 14 nm silicon geometry (shown in Figure 1). Now offered in the Gen3 revision, it includes eight 14-bit ADCs sampling at 5 GS/sec capable of direct RF digitization of input signals up to 6 GHz, and eight 14-bit DACs sampling at 9.8 GS/sec. These data converters are connected directly to the Zynq FPGA fabric, eliminating the power, connections, complexity, and latencies of external interfaces to discrete data converters. An onboard, multicore Arm processor serves as a system controller, providing control, status, I/O, and a 1 GbE interface to an external host. Two 100 GbE interfaces connect the RFSoC to external devices supporting 24 GB/sec data transfers in both directions. (Figure 1.)



[Figure 1 | Xilinx's Zynq UltraScale+ RFSoC Gen3 device combines all critical components of of EW subsystem including eight RF ADCs and DACs, high-speed Ethernet and PCIe, DDR4 SDRAM interfaces, and multicore Arm processors.]

Targeting the massive-MIMO antenna requirements of 5G commercial wireless, RFSoC supports key functions for 8-elements of a phased array including direct transmit/receive RF conversion, real-time DSP, and control. By effectively addressing so many tough requirements, this new FPGA architecture was immediately attractive to EW designers. Its small size not only reduces SWaP-C, especially critical for air vehicles and small EW countermeasure systems, but it also enables new system architectures that provide significant performance enhancements.

This technology enables compact small-form-factor (SFF) enclosures holding RF circuitry to convert antenna signal frequencies to-and-from L-band along with the RFSoC devices, to be integrated within or behind the antenna array. Inside the RFSoC, digital lines from the data converters connect directly into the FPGA fabric, drastically reducing latency compared to external discrete devices with serial JESDS204 interfaces. DSP functions within the FPGA can locally apply the required phase shifts to the elements for beam steering receive and transmit signals, and handle signal acquisition, triggering, waveform generation, time stamping, digital up/down conversion. These real-time front-end operations can significantly off-load backend processing tasks. (Figure 2.)

[Figure 2 | This RFSoC-based small-form-factor ruggedized subsystem provides eight channels of remote data acquisition and generation, local Arm processor system controller, FPGA fabric for DSP, and dual 100 GbE optical interfaces with VITA-49 data protocol.]

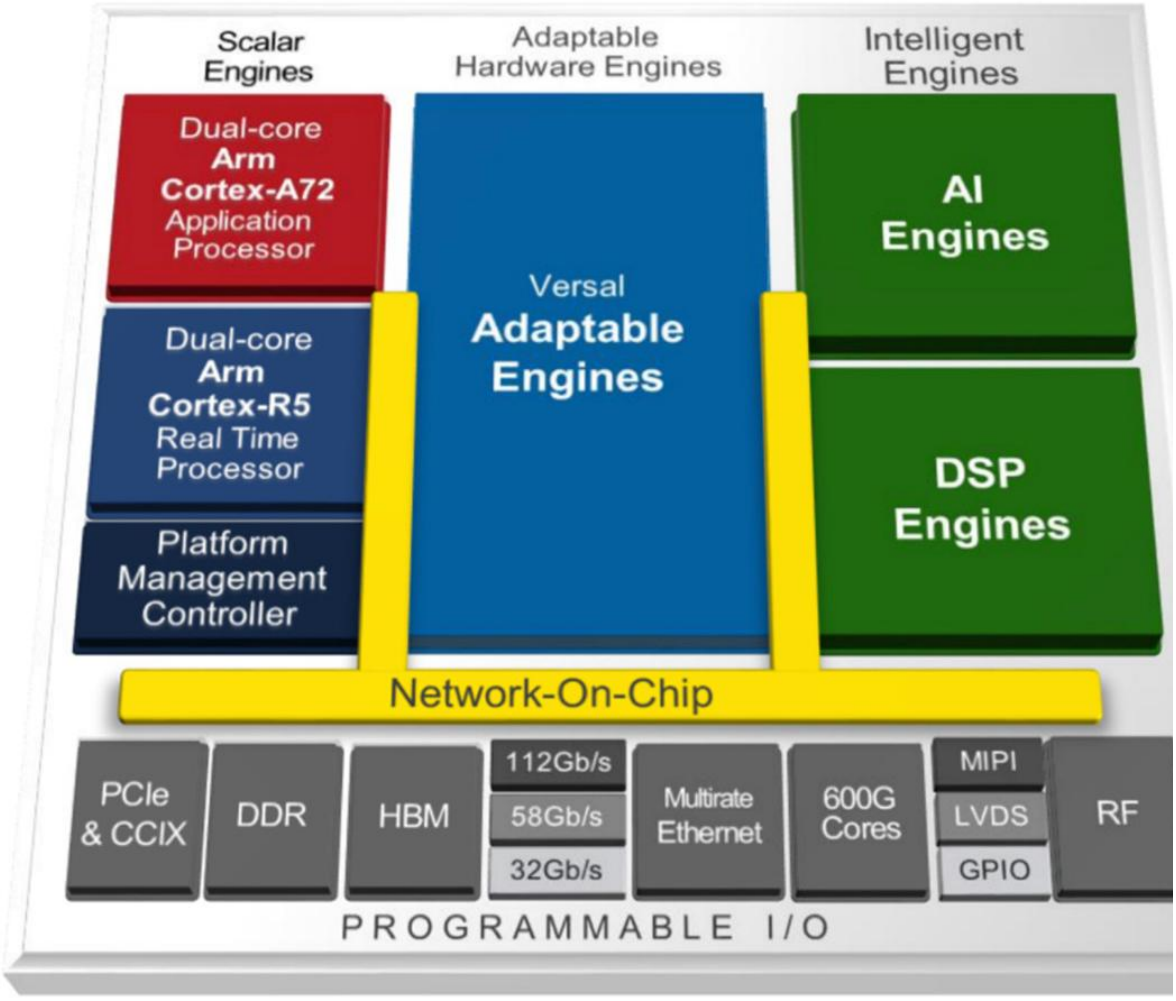
Sensitive RF circuitry and data converters are now inside the SFF enclosure, eliminating the need for long analog RF cables and their many disadvantages. Instead, digitized payload signals can be connected to the host system using gigabit serial links, a popular trend for embedded system interconnections. Once again, the RFSoC steps up to the task by providing two 100 GbE interface engines, each supported with four full-duplex 25 Gbaud lanes.

By equipping each subsystem with optical transceivers, multimode fiber optical cables can deliver data at 24 GB/sec across distances as far as 100 meters. These links are not only lighter, smaller, and less expensive than RF cables, but they are also impervious to electromagnetic interference so as to maintain full signal integrity.

Because RFSoC offers a complete software radio subsystem on a chip, it opens a wealth of new EW uses previously impractical with earlier technology. These include small standalone monitoring stations, smarter munitions, more agile countermeasure and fire-control systems, and better troop protection.

Next-generation devices for EW

Xilinx's latest offering is the Versal ACAP [adaptive compute acceleration platform] family of hardware devices and supporting development tools. Different members of the family provide different blends of three major processing resources: scalar processors (ARM CPUs), adaptable logic (FPGAs), and vector processors (GPUs and DSPs), as shown in Figure 3. These last two resources support AI capabilities such as inference, image processing, pattern recognition, and signature detection, all of which are extremely appropriate for EW as well as for many other defense applications. One even offers onboard direct sampling RF ADCs and DACs, following the successful theme introduced by RFSoC.



[Figure 3 | Xilinx Versal AI ACAP (Adaptive Compute Acceleration Platform) heterogeneous processor includes blends of DSP engines, artificial intelligence (AI) engines, adaptable FPGA engines, multicore Arm processors, network-on-chip, high bandwidth and DDR memories, multirate Ethernet I/O, and RF I/O (courtesy Xilinx).]

This heterogenous mix of ACAP resources gives designers the freedom to assign compute power to the processing engine most suitable to the task at hand, and the ability to adaptively reassign resources as required. This flexibility of ACAP delivers as much as ten times the performance over dedicated processor types alone.

Onboard, flexible high-bandwidth memory (HBM) and fast DDR4 SDRAM structures eliminate the need for external devices. To interconnect these resources, ACAP includes an extremely wideband, configurable network-on-chip that offers a uniform interface and protocol to simplify system integration.

Versal development tools target high-level design entry from frameworks, models, C language, and RTL coding. Users can create a custom development environment to suit their project needs and programming preferences. Other Versal hardware/software platforms will evolve to help speed EW development tasks and support high complexity and extreme performance requirements.

Looking forward

Several clear trends for EW are evident: Integrating data converters and processors into a single device solves several critical problems in the areas of system architecture, performance levels, and costs. Combining data converters with a single type of signal processor is a good start, but a heterogeneous mix of specialized processing resources means that a common platform can support a wider range of deployment scenarios and applications.

Lastly, harnessing this new complex technology requires development tools supporting high-level design entry and flexible migration of tasks across the many resources. Expect ongoing development of these technologies to meet the evolving EW needs of warfighters.

Rodger Hosking is vice president of Mercury Microelectronics, a wholly owned subsidiary of Mercury Systems (formerly Pentek). With more than 30 years in the electronics industry, he has authored hundreds of articles about software radio and digital signal processing. Prior to his current position, he served as engineering manager at Wavetek/Rockland; he also holds patents in frequency synthesis and spectrum-analysis techniques. He holds a BS degree in physics from Allegheny College in Pennsylvania and BSEE and MSEE degrees from Columbia University in New York.

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MERCURY SYSTEMS
50 Minuteman Road
Andover, Massachusetts 01810
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sales@mrcy.com

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1 Park Way
Upper Saddle River, NJ 07458
Website
sales@pentek.com
201-818-5900

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