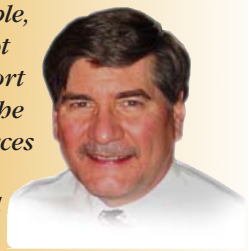
The Pentek Pipeline
A quarterly publication for engineering system design and applications.

Fall 2009 • Vol. 18, No. 3

Pentek, Inc.
One Park Way, Upper Saddle River, NJ 07458
Tel: (201) 818-5900 • Fax: (201) 818-5904
email: pipeline@pentek.com
http://www.pentek.com

In This Issue

"Because they are configurable, FPGAs not only support many of the key resources on our board-level products, they also help extend product life cycles."



Rodger Hosking, Pentek Vice President and Cofounder

Free Technical Resources

New edition of the *High-Speed Switched Serial Fabrics Handbook:* pentek.com/go/pipeserhb

New edition of the *SDR Handbook:* pentek.com/go/pipesdrhb

New edition of the *FPGAs for Software Radio Systems Handbook:* pentek.com/go/pipefpgahb

New edition of the *High-Speed A/Ds Handbook:* pentek.com/go/pipecrithb

Virtex-6 FPGAs Push the Performance Envelope

With each new generation of FPGA devices, Xilinx continues to push the performance envelope to match the ever increasing requirements of target applications. The recent announcement of the Virtex-6 family is no exception. More processing power, lower power consumption and updated interface features to match the latest technology I/O requirements are all part of the new devices.

While it might be easy to assume that faster, bigger, more powerful is better, it's important to understand how the latest FPGA innovations actually deliver this higher performance to best match the device to the specific requirements of the application.

Depending on how you interpret the Xilinx naming conventions, the Virtex-6 is the fifth or sixth generation of devices—'Virtex-3' was skipped over. Of these families, Virtex-4, Virtex-5 and, of course, Virtex-6 are all viable processing platforms; they are worth comparing, so that one can understand the progression of increasing performance culminating in the latest generation.

Logic Cells, Slices and CLBs

Virtex FPGAs follow a naming convention that includes the size of the device in the name. Specifically the approximate number of **Logic Cells** contained in the part is included in the part number. For example a Virtex-6 LX240T device contains approximately 240,000 Logic Cells, while a Virtex-5 SX95T contains approximately 95,000 Logic Cells. Sounds simple, and it is, but just comparing the amount of Logic Cells can be misleading.

Logic Cells consist of combinational logic that creates a lookup table which implements functions such as AND, OR, NAND, and addition. Flip flops and the connections to the adjacent cells are also implemented in the Logic Cell. Multiple Logic Cells are grouped together to create a single unit, called a **Slice**. As the architecture of the Virtex has evolved, the number of Logic Cells in a Slice has changed: a Virtex-4 Slice consists of two Logic Cells, Virtex-5 and Virtex-6 Slices consist of six Logic Cells.

The next step up on the architectural hierarchy is the **CLB** (Configurable Logic Block). Here again, the development of more powerful CLBs has changed the relationship between Slices and CLBs: a Virtex-4 CLB consists of four Slices and Virtex-5 and Virtex-6 CLBs consist of two Slices. As a result, Virtex-4 CLBs require eight Logic Cells and Virtex-5 or Virtex-6 require 12 Logic Cells. Figure 1 compares these parameters in the three Xilinx generations.

So why did Xilinx design FPGA logic in this hierarchical organization instead of just creating

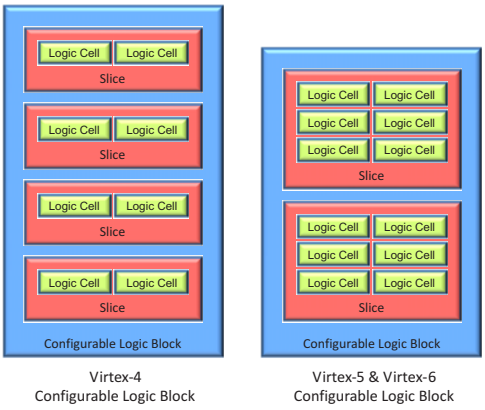


Figure 1. CLB Comparison, Virtex-4 vs. Virtex-5 and Virtex-6 FPGAs

a flat plane of interconnected Logic Cells? The multilevel design of modern FPGA devices creates a balance between interconnect speed and interconnect flexibility. The fastest connections exist between Logic Cells. Connections between Slices are slower and connections between CLBs are even a little slower. Going in the other direction, connections between CLBs are the most flexible and general purpose, Slice connections are a bit less flexible, and connections between Logic Cells are more limited.

Increasing Density

With each new generation of FPGAs, comes higher component density in the form of more Logic Cells. Figure 2 graphs the Logic Cell densities of various devices from the last three Virtex generations. For each generation, Xilinx offers a range of different density devices within a ➤

Virtex-6 FPGAs Push the Performance Envelope

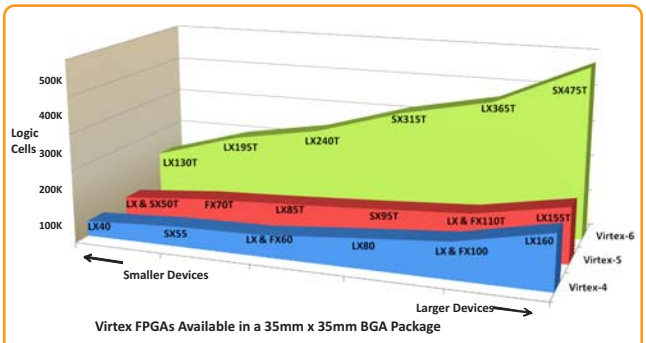


Figure 2. Logic Cell Density Comparison, Virtex-4, Virtex-5 and Virtex-6 FPGAs

➤ single package type. To focus the scope of this comparison, all of the devices compared are available in the same 35 mm x 35 mm BGA (Ball-Grid Array) package.

Since Virtex-4 CLBs comprise eight Logic Cells, while Virtex-5 and Virtex-6 CLBs comprise 12, the increase in Logic Cells between Virtex-4 and Virtex-5 actually translates to a decrease in CLBs because each CLB in the Virtex-5 requires more Logic Cells. While the Virtex-5 CLBs are more powerful than their Virtex-4 counterparts, there are still fewer of them to use. What is also clear from this graph is that the Virtex-6 represents a significant increase in density from the Virtex-5 family.

Geometries, Speed and Power

So how are more Logic Cells packed into the same size package with each new generation? As you might expect, by shrinking the physical size of the logic. IC geometries are measured in nm (nanometers). The progression from Virtex-4 through Virtex-6 has been from 90 nm to 65 nm to 40 nm. An additional benefit of shrinking transistors is an increase in switching rates which translates to faster clock speeds. Virtex-4 runs at 500 MHz, Virtex-5 runs at 550 MHz and Virtex-6 achieves a 600 MHz clock rate.

Unfortunately, whether it's lunch or shrinking transistors, nothing comes for free. Leakage current tends to increase exponentially as the transistors shrink, increasing the static power, even when the transistors aren't switching. To compensate, Xilinx has introduced a series of power saving design techniques. Depending on the mode the FPGA is operating, a power savings of between 20% and 40% can be achieved on the Virtex-6 when compared to comparable Virtex-4 devices. Again, as densities increase and more Logic Cells are packed in the same size device, these power savings become imperative.

DSPs and Memory

In addition to CLBs, Virtex FPGAs contain DSP Slices. These are dedicated multipliers, multiply-accumulator or multiply-adder blocks. The DSP slices are responsible for the majority of the processing horsepower of FPGAs. Like the CLBs, the DSPs benefit from a compound performance increase with each new generation: improvements in the actual DSP logic; increases in operational speed from 500 MHz to 550 MHz to 600 MHz with the latest generation; and increasing density allowing more DSP slices to be included in the same size package. While the largest Virtex-4 device includes 512 DSP Slices, the Virtex-6 tops out at an impressive 2016.

All Virtex FPGAs include integrated memory blocks (Block RAM) for implementing anything from random access storage to dual-port architectures, to FIFOs — depending on the application. For the 35 mm x 35 mm package we've been comparing, Block RAM has increased from a maximum of approximately 7 megabits to 8 megabits between the Virtex-4 and Virtex-5; it then took a sizable leap to a maximum of 38 megabits for the Virtex-6.

Connecting it all together

Through the last few generations of Virtex devices, BGA ball pitch has remained the same at 1 mm, which means there is 1 mm spacing between the BGA balls. In a 35 mm x 35 mm device, this turns out to be between 1136 and 1152 pins, depending on the device. Because of this, I/O density hasn't really seen an increase, but the number of different I/O signal types has been expanded as well as I/O speed. The general purpose I/O, *SelectIO*, is used for connecting everything from devices like A/Ds and D/As, creating parallel data buses, or implementing memory interfaces. The Virtex-6 family is compatible with the latest QDRII+ and DDR3 technology and Xilinx provides examples for implementing interfaces to these devices.

A key interface feature of all of the current Virtex generations is gigabit serial transceivers. Originally named *RocketIO* and now *GTX transceivers*, these provide an essential high-speed interface for moving data on and off the FPGA. Like the *SelectI/O*, *GTX transceivers* have remained similar in number, a maximum between 16 and 20 on the 35 mm square devices we've been comparing. These interfaces can be used to implement different protocols, such as *Serial RapidIO* and Xilinx's own *Aurora*, a license-free, lightweight protocol ideal for fast point-to-point data connections.

With *PCI Express* rapidly becoming more prevalent in systems from desktop PCs to targeted digital signal processing subsystems, Xilinx has included integrated *PCI Express* cores designed to support the gigabit serial transceivers. Virtex-6 supports *PCI Express* Base Specification 2.0 in x1 through x8 configurations.

As Figure 3 shows, each new generation of FPGAs is enabled by a range of technical advances. These span broad improvements like power reduction and device density to the intricacies of data pipelining and the addition of a single strategically placed flip-flop in the CLB that an experienced FPGA engineer will exploit to the fullest. But even from just looking at the few metrics compared in this article, it's easy to see the ongoing progression of FPGA technology and why FPGAs continue to be a preferred platform for digital signal processing. ❑

Virtex devices available in a 35 mm x 35 mm BGA package			
Resource	**Virtex-4***	**Virtex-5***	**Virtex-6***
Logic Cells	41K – 152K	46K – 156K	128K – 476K
Slices**	18K – 68K	7K – 24K	20K – 74K
CLBs	4608 – 16896	3600 – 12160	10000 – 37200
Block RAM (kb)	1728 – 6768	2160 – 8784	9504 – 38304
DSP Slices	64 – 512	48 – 640	480 – 2016
Serial Transceivers	0 – 20	12 – 16	20
SelectIO	448 – 768	480 – 640	600

* Virtex-4 FX, LX, and SX devices; Virtex-5 FXT, LXT and SXT devices; Virtex-6 LXT and SXT devices
** Virtex-4 Slices actually require 2.25 Logic Cells and Virtex-5 and Virtex-6 Slices actually require 6.4 Logic Cells

Figure 3. Resource Comparison, Virtex-4, Virtex-5 and Virtex-6 FPGAs

Product Focus
Series 7800

Pentek Announces The New Series 7800 Software Radio Half-Length x8 PCIe Boards

Routing flexibility designed for communications, software radio, telemetry, and signal intelligence applications

Model 7841 Dual Multiband Transceiver with FPGA

Features

- Gen. 2 PCIe, x8 wide
- Two 125 MHz, 14-bit A/Ds
- Four-channel DDC (Downconverter)
- One DUC (Upconverter)
- Two 500 MHz, 16-bit D/As
- One Xilinx Virtex-II Pro FPGA
- 512 MB DDR SDRAM
- LVDS clock/sync bus for multiboard synchronization
- Datasheet: pentek.com/go/pipe7841

Model 7842 Multichannel Transceiver with FPGAs

Features

- Gen. 2 PCIe, x8 wide
- Four 125 MHz, 14-bit A/Ds
- One DUC (Upconverter)
- One 500 MHz, 16-bit D/A
- Two Xilinx Virtex-4 FPGAs
- 768 MB DDR2 SDRAM
- LVDS clock/sync bus for multiboard synchronization
- Optional factory-installed DDC cores
- Datasheet: pentek.com/go/pipe7842

Model 7850 Quad 200 MHz, 16-bit A/D with FPGAs

Features

- Gen. 2 PCIe, x8 wide
- Four 200 MHz, 16-bit A/Ds
- Two Xilinx Virtex-5 FPGAs
- 1.5 GB DDR2 SDRAM
- LVPECL clock/sync bus for multiboard synchronization
- Optional factory-installed DDC cores
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O
- Datasheet: pentek.com/go/pipe7850

Model 7851 256-Channel DDC, four 200 MHz A/Ds

Features

- Gen. 2 PCIe, x8 wide
- 256 channels of DDCs in four banks
- Independent tuning for each channel
- DDC decimation from 128 to 1024
- User-programmable 18-bit FIR filter coefficients
- Four 200 MHz, 16-bit A/Ds
- LVPECL clock/sync bus for multiboard synchronization
- Datasheet: pentek.com/go/pipe7851

Model 7852 32-Channel DDC, four 200 MHz A/Ds

Features

- Gen. 2 PCIe, x8 wide
- 32 channels of DDCs in four banks
- Independent tuning for each channel
- DDC decimation from 16 to 9192
- User-programmable 18-bit FIR filter coefficients
- Power meters and threshold detectors
- LVPECL clock/sync bus for multiboard synchronization
- Datasheet: pentek.com/go/pipe7852

Model 7856 Dual 400 MHz A/D and 800 MHz D/A

Features

- Gen. 2 PCIe, x8 wide
- Two 400 MHz, 14-bit A/Ds
- One DUC (Upconverter)
- Two 800 MHz, 16-bit D/As
- Independent A/D and D/A clocks
- Two Xilinx Virtex-5 FPGAs
- 1 GB DDR2 SDRAM
- LVPECL clock/sync bus for multiboard synchronization
- Datasheet: pentek.com/go/pipe7856

PCI EXPRESS™

PCI EXPRESS™

Product Focus

Model 7156

New Software Radio PMC/XMC Captures and Processes Wideband Signals

Model 7156 is also available in PCI, PCIe and cPCI formats

ReadyFlow Board Support Package GateFlow

Features

- Two 400 MHz, 14-bit A/Ds
- One digital upconverter
- Two 800 MHz, 16-bit D/As
- Up to 1 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Dual timing buses for independent A/D and D/A clock rates
- LVPECL clock/sync bus for multimodule synchronization
- VITA 42.0 XMC compatible with switched fabric interfaces
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O on P14

General Information

Model 7156 is a dual-channel, high-speed data converter suitable for connection to HF or IF ports of a communications system. It includes two A/D and two D/A converters, two Virtex-5 FPGAs and two banks of DDR2 SDRAM. The Model 7156 uses the popular PMC format and supports the VITA 42 XMC standard for switched fabric interfaces.

A/D Converter

The front end accepts two full-scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into TI ADS5474 14-bit 400 MHz A/Ds. Designed with a 750 MHz input bandwidth, the A/Ds are excellent for undersampling applications.

The digital outputs are delivered to the Virtex-5 FPGA for signal processing, data capture or routing to other module resources.

Digital Upconverter and D/A

A TI DAC5688 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 300 MHz. It delivers real or quadrature (I+Q) outputs at up to 500 MHz to the 16-bit D/A converter. Analog output is through a pair of front panel SMC connectors at +4 dBm into 50 ohms. If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2, 4, and 8.

Virtex-5 FPGAs

The Model 7156 architecture includes two Virtex-5 FPGAs. The processing FPGA serves as a control and status engine with data and programming interfaces to all of the on-board resources.

A second Virtex-5 FPGA provides the board's PCI-X interface. Implementing the interface in this second FPGA keeps the processing FPGA resources free for signal processing.

Option -104 adds the P14 PMC connector with 16 pairs of LVDS connections to each FPGA for custom I/O.

XMC Interface

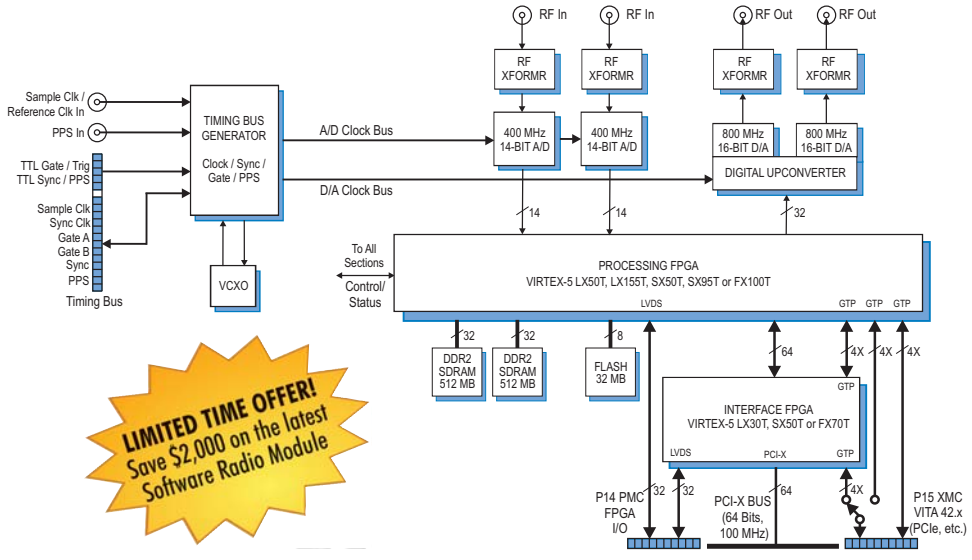
The Model 7156 complies with the VITA 42.0 XMC specification for carrier boards. This standard provides, among others, for a x4 link with a 3.125 GHz bit clock between the XMC module and the carrier board. With two x4 links, the 7156 achieves 2.5 GB/sec streaming data transfer rate independent of the PCI interface and supports switched fabric protocols such as Serial RapidIO and PCI Express

Clocking and Synchronization

Two internal timing buses can provide either a single clock or two different clock rates to the A/D and D/A signal paths.

A front panel LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

For more information and a special "sales bundle": pentek.com/go/pipe7156B. ❑



Product Focus

Model 7190

Multifrequency Clock Synthesizer PMC Module

Model 7190 is also available in PCI, PCIe and cPCI formats

ReadyFlow Board Support Package

Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources with typical phase noise of –125 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal of 5 or 10 MHz
- Four quad VCXOs allow selection from 16 different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 500 MHz

General Information

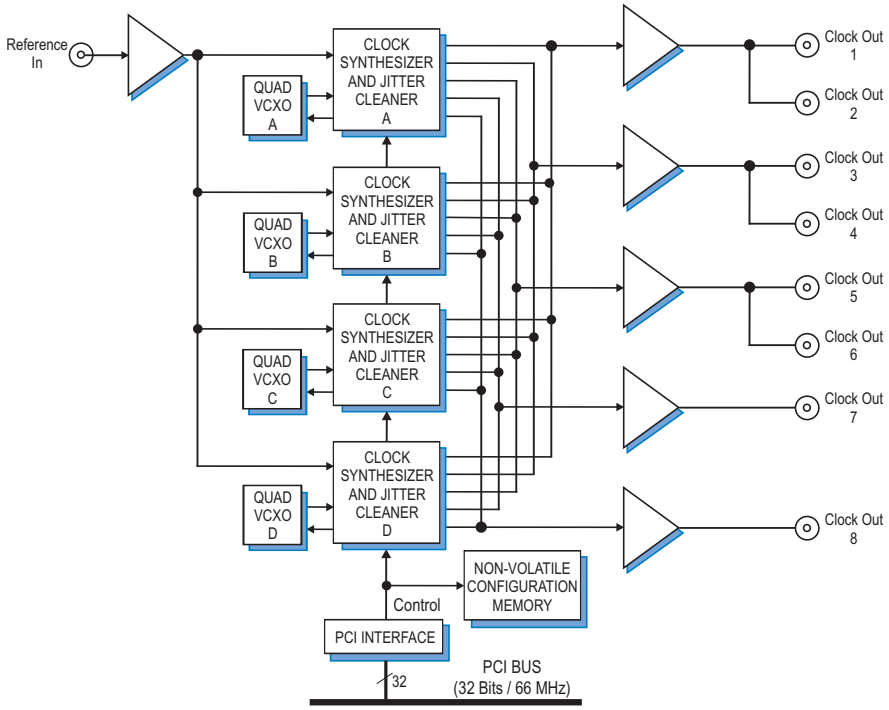
Model 7190 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from an input reference signal using phase-locked oscillators.

Clock Synthesizer Circuits

The 7190 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 includes phase-locking circuitry that locks the frequency of its associated quad VCXO (Voltage Controlled Crystal Oscillator) to the input reference clock. This reference is a 5 or 10 MHz signal supplied to a front panel SMC connector. Each quad VCXO is programmed to generate one of four base frequencies.

Each CDC7005 generates five output signals. Each signal is independently programmable as a submultiple of the associated VCXO base frequency using divisors of 1, 2, 4, 8 or 16.

The five clock output signals from each of the four CDC7005s are joined into five clock buses. Each CDC7005 output can be independently enabled to drive each bus, thereby allowing any combination of output signals from the four CDC7005s.



Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock buses, as shown in the block diagram. This supports a single identical clock to all eight outputs or five different clocks to various outputs; numerous other combinations are possible.

PCI Interface

The Model 7190 uses an industry-standard 32 bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the module.

Power Up Auto Configuration

The 7190 is equipped with a non-volatile memory. Once configured, the settings return to the saved configuration upon power up. Once a configuration is saved, the 7190 does not require PCI access; this is convenient for deployed applications that do not include a host computer.

For more information including options, such as frequencies of factory-installed VCXOs, and price quotation on the Model 7190, please go to:

pentek.com/go/pipe7190. ❑

Product Focus

Model RTS 2721

Portable Real-Time Multiband Recording and Playback Instrument

General Information

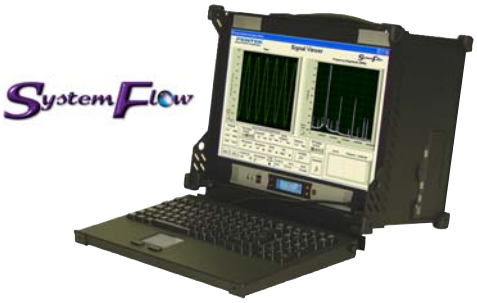
The Pentek RTS 2721 is a turnkey, multiband recording and playback instrument that allows the user to record and reproduce high-bandwidth signals with a lightweight, portable package. The instrument provides sustained recording and playback rates of up to 480 MB/sec in a dual-channel system and is ideal for the user who requires both portability and power in a recording system.

The RTS 2721 is supplied in a small footprint portable package measuring only 16.9" W x 9.5" D x 13.4" H and weighing just 30 pounds. With measurements similar to a small briefcase, this portable workstation includes a quad-core Xeon processor, a high-resolution 17" LCD monitor, and a high-performance SATA RAID controller.

The heart of the RTS 2721 is the Pentek Model 7641-420 multiband transceiver which includes recently introduced A/D and D/A converters, DDCs (digital downconverters), DUCs (digital upconverters), and complementary FPGA IP cores. This architecture allows the system engineer to take full advantage of the latest technology in a turnkey instrument.

Features

- Lightweight: approximately 30 lbs
- High-performance Windows® workstation
- Two 14-bit 125 MHz A/Ds
- One 16-bit 500 MHz D/A
- Real-time sustained recording rates of up to 480 MB/sec
- Standard configuration with 3 TB of hot-swap storage to NTFS disk array
- RAID levels 0 ,1, 5 , 6, 10 and 50
- Windows SystemFlow® instrument software
- Complete GUI with Signal Viewer analysis tool that includes a virtual oscilloscope and spectrum analyzer
- DDC decimation and DUC interpolation range from 2 to 32,768
- 8 kHz to 60 MHz baseband record and playback signal bandwidths
- Ideal for communications, radar, wireless, SIGINT, telecom and satcom

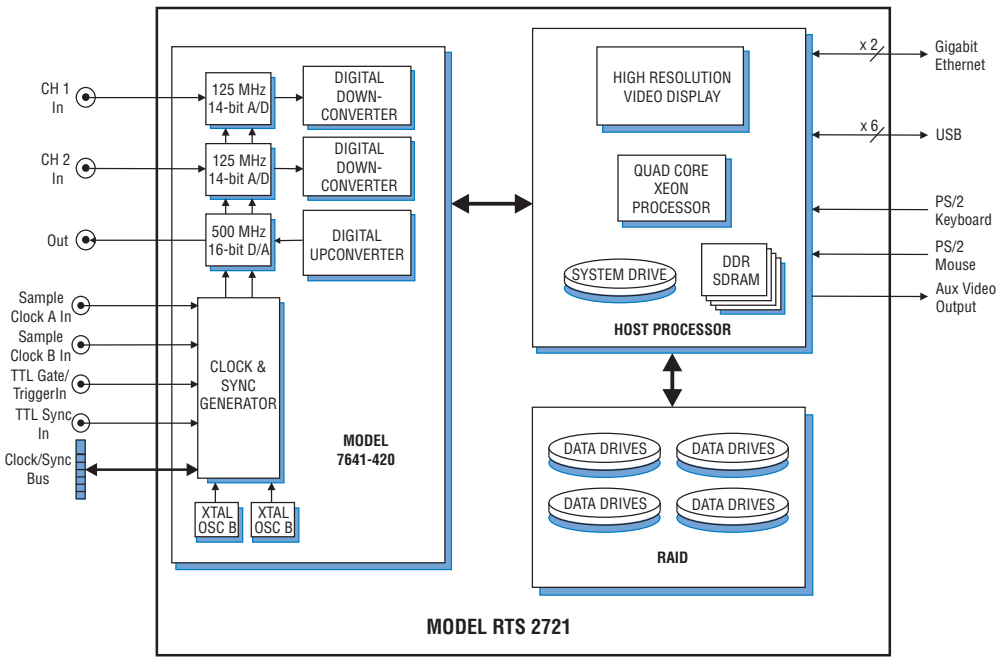


SystemFlow Software

Fully supported by Pentek's Model 4990 SystemFlow instrument software, the RTS 2721 features a Windows-based GUI (graphical user interface) that provides a simple means to configure and control the instrument. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows XP Professional workstation, the instrument allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2721 records data to the native NTFS file system that provides immediate access to the recorded data. Data can be offloaded via the hot-swap SATA disks, by gigabit Ethernet or USB 2.0.



Flexible Architecture

Pentek's portable multiband recorder provides a flexible architecture that is easily customized to meet the user's needs. Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the level of redundancy that's required. Total drive capacity is scalable up to 4.8 TB using as many as 14 hot-swap SATA drives.

The system supports simultaneous recording of one or two wideband A/D or multiband DDC channels. The analog output allows a single recorded signal to be reproduced as either a baseband signal or an upconverted IF signal. With its wide range of programmable decimation and interpolation factors, the system supports signal bandwidths from 8 kHz to 60 MHz.

For more information including options and price quotation on the Model RTS 2721, please go to: pentek.com/go/pipe2721. ❑

Product Focus

Model RTS 2701

Rack-Mount Real-Time Data Recording and Playback System with Multiband Transceiver

Features

- 19 inch industrial rack-mount PC server chassis
- High-performance Windows® workstation
- Two 14-bit 125 MHz A/Ds
- Two 16-bit 500 MHz D/As
- Real-time sustained recording and playback rates up to 500 MBytes/sec
- 5 TB storage to NTFS RAID disk array
- RAID levels 0 ,1, 5 , 6, 10 and 50
- Pentek SystemFlow® recording and playback software
- Signal Viewer analysis tool includes virtual oscilloscope and spectrum analyzer ➤
- DDC decimation and DUC interpolation range from 2 to 32,768
- 8 kHz to 60 MHz baseband record and playback signal bandwidths
- Ideal for communications, radar, wireless, SIGINT, telecom and satcom

General Information

The Pentek RTS 2701 is a turnkey, multiband recording and playback system that allows the user to record and reproduce high-bandwidth signals. The RTS 2701 provides sustained recording and playback rates of up to 500 MB/sec in a dual-channel system and is ideal for the user that requires a powerful rack-mount recording system.

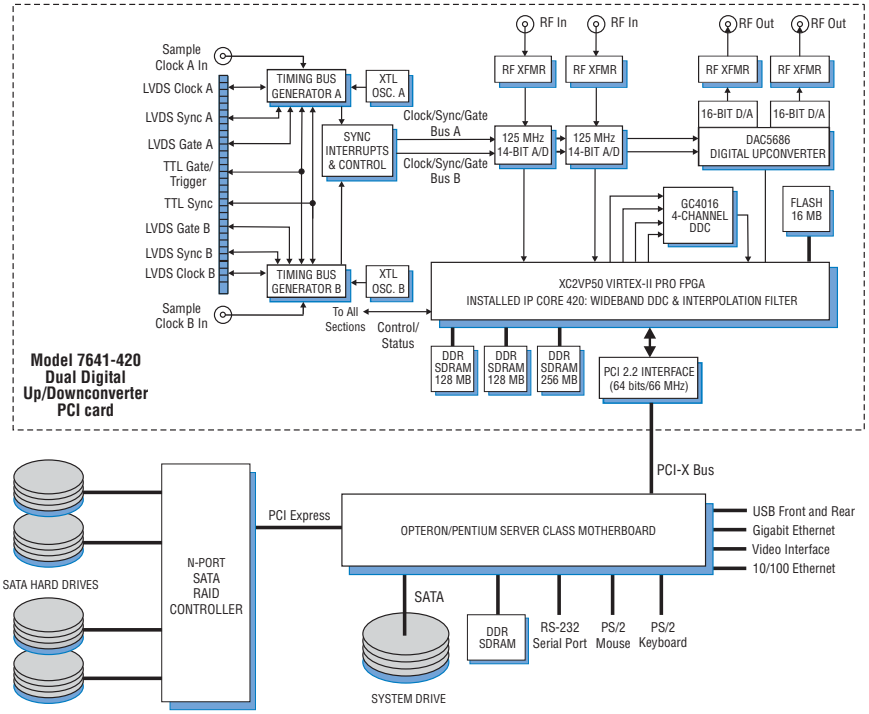
The heart of the RTS 2701 is the Pentek Model 7641-420 multiband transceiver which includes recently introduced A/D and D/A converters, DDCs (digital down-converters), DUCs (digital upconverters), and an FPGA-installed IP core. The architecture allows the system engineer to take full advantage of the latest technology in a turnkey system.

SystemFlow Software

Fully supported by Pentek's Model 4990 SystemFlow Recording Software, the RTS 2701 features a Windows-based GUI (graphical user interface) that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select pre-configured settings with a single click.

SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows XP Professional workstation, users can install post-processing and analysis tools to operate on the recorded data. The RTS 2701 records data to the native NTFS file system thereby providing immediate access to the recorded data. Data can be offloaded via gigabit Ethernet, or USB 2.0 ports. Additionally, data can be copied to disk, using the 8X double layer DVD +–R/RW drive.



Flexible Architecture

Pentek's multiband recorder system provides a flexible architecture that is easily customized to meet the user's needs. Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the level of redundancy that's required. Total drive capacity is 5 terabytes using ten drives.

The system supports simultaneous recording of one or two wideband A/Ds or multiband DDC channels. Two analog outputs allow recorded signals to be reproduced as either two baseband signals or one upconverted IF signal. With its wide range of programmable decimation and interpolation, the system supports signal bandwidths from 8 kHz to 60 MHz.

For more information including options, number and type of analog channels, recording rates, disk capacity, and price quotation on the Model RTS 2701, please go to pentek.com/go/pipe2701. ❑