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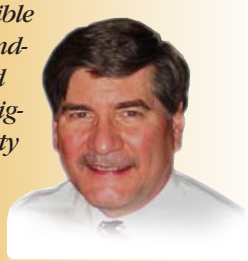
Pentek, Inc.
One Park Way, Upper Saddle River, NJ 07458
Tel: (201) 818-5900 • Fax: (201) 818-5904
email: pipeline@pentek.com
http://www.pentek.com

In This Issue

- FPGA-based DDCs have become a cornerstone technology in communication systems. More in the feature article.

"Radically new DDC architectures targeting maximum channel count, flexible channel bandwidth and improved signal integrity are now possible because of the growing wealth of DSP resources in the latest FPGAs."



Rodger Hosking, Pentek Vice President and Cofounder

- **Product Focus:** Model 7152 32-channel DDC Click here

- **Product Focus:** Model 7153 4- or 2-channel DDC. Click here

Technical Resources

Download the 1st edition of the *High-Speed Switched Serial Fabrics Handbook:*
pentek.com/go/pipeserhb

Download the 6th edition of the *Digital Receiver Handbook:*
pentek.com/go/pipedrhb

Download the 3rd edition of *FPGAs for Software Radio Handbook:*
pentek.com/go/pipefpgahb

Download the 2nd edition of *Critical Techniques for High-Speed A/D Converters in Real-Time Systems:*
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Features and Benefits of FPGA-Based DDCs

The DDC (Digital Downconverter) has become a cornerstone technology in communication systems. Similar to its analog receiver counterpart, the DDC provides the user with a means to tune and extract a frequency of interest from a broad radio spectrum. Over the past few years, the functions associated with DDCs have seen a shift from being delivered in ASICs (Application-Specific ICs) to operating as IP (Intellectual Property) in FPGAs (Field-Programmable Gate Arrays).

For many applications, this implementation shift brings advantages that include: design flexibility, higher precision processing, higher channel density, lower power, and lower cost per channel. With the advent of each new higher performance FPGA family during the past few years, these benefits continue to increase.

In this article, we will explore some of the key advantages of implementing DDC designs in FPGAs and will describe some of the situations when ASICs can still offer the best solution.

Digital Downconverter Fundamentals

To understand how FPGAs play a key role in implementing DDCs that perform the function of a receiver, it's important to break the DDC down into its individual functional blocks. Figure 1 shows a classic DDC. Regardless of whether it's implemented in an ASIC or an FPGA, this is the common architecture of the DDC function.

The first stage of the DDC uses a complex digital mixer to translate the frequency of interest down to baseband. It uses a pair of multipliers and a DDS (Direct Digital Synthesizer) as the NCO (Numerically Controlled Oscillator). This function enables the user to tune the receiver to the desired frequency of interest. The second stage of the DDC reduces the sampling frequency of the signal to match the desired output bandwidth. It uses a CIC (Cascaded Integrator Comb) filter to decimate the data.

A second CIC filter provides a coarse gain adjustment stage. The signal is then passed to a pair of additional polyphase filters. First a CFIR (Compensation Finite Impulse Response) filter then to a PFIR (Programmable Finite Impulse Response) filter. This filter pair provides additional decimation and final signal shaping prior to the rounding stage and final output.

When we get past all the acronyms, we realize that most of the individual function blocks of the DDC are implemented using multipliers. It thus becomes apparent how the DDC might map into current FPGA families. Most new FPGAs include a wealth of DSP function blocks which are primarily multipliers. The general purpose logic resource and on-chip memory of FPGAs also match the requirements of the DDC for implementing the required FIR filters and filter coefficient tables. ➤

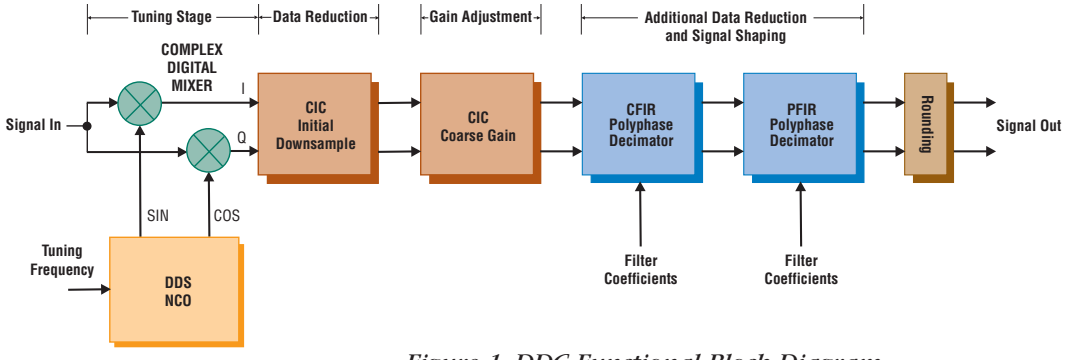


Figure 1. DDC Functional Block Diagram.

Features and Benefits of FPGA-Based DDCs

DDCs as Intellectual Property Cores

As part of their IP (intellectual property) library series, Xilinx provides a free DDC core. The core serves as a good general reference design, following the classic DDC architecture shown in Figure 1. While this core can be used as a building block for general purpose DDCs, the real advantages of an IP-based implementation can be best seen in optimized custom cores that are designed to match the requirements of a specific application.

IP Enables Software Radio Products

Pentek offers a series of high-performance IP- based DDCs, available preinstalled in software radio modules. Each is optimized to match a specific range of application requirements.

These cores range from the high-channel count/narrow bandwidth of the 430 Core installed in the Model 7141, to the wider bandwidths and excellent SFDR (Spurious Free Dynamic Range) of the core installed in the Model 7153.

Table 1 lists the range of DDC cores available from Pentek as software radio modules. For each core, pertinent specifications are listed. All products are available in industry standard PMC/XMC modules as well as 3U and 6U CompactPCI, PCI and PCI Express form factors. In addition to the IP-based solutions, a popular ASIC-based DDC solution from Texas Instruments, the GC4016, is included as a reference.

When compared on a size/power/cost per channel basis, it becomes apparent that narrowband, high channel-count DDC cores can be very efficiently implemented in FPGAs. Implementation of wideband DDCs consumes many more FPGA DSP and logic resources. As a result, the number of channels that can be fit into a single FPGA is limited. Even with less cost-effective wideband DDCs, the custom IP approach can sometimes provide the only viable solution when a specific performance characteristic is required. The improved SFDR of the Pentek 420 core is an example of such a requirement.

Flexible Implementation

An additional benefit of IP based solutions is the flexible nature of their implementation. The Models 7141-420 and 7141-430 are created by using the same hardware base with different installed IP cores. Similarly, the Models 7151, 7152 and 7153 are all based on the same 4-channel, 200 MHz, 16-bit A/D PMC/XMC with different FPGA IP cores. All share the same software base allowing migration between different applications to be accomplished with minimum software porting.

Additionally, some applications like JTRS (Joint Tactical Radio System), need to operate across a wide spectrum to handle the diverse signal types. Such applications can benefit greatly by IP based solutions. Figure 2 on the next page, shows the six optimized Pentek cores across a range of applications and the number of channels and bandwidth they typically require.

Again, this wide range of applications can be satisfied by using a small set of hardware with different, optimized IP cores. This is one of the fundamental concepts of SDR (Software Defined Radio), and it's difficult, if not impossible, to achieve with ASIC-based solutions. ➤

DDC Implementation	Number of Channels	Decimation Range	Input Rate (MHz)	SFDR (dBFS)	Decimation Steps	Area per Channel (mm²)[1]	Power per Channel (W)[2]	Cost per Channel ($)[3]
TI GC4016 ASIC	4	32–16,384	160	115	1	72.3	0.25	41
Pentek 7141-420	2	2–64	110	118	Binary	612.5	2.5	204
Pentek 7141-430	256	1,024–9,984	110	110	256	4.7	0.01	2
Pentek 7142-428	4	2–65,536	125	108	1	206.2	2.0	102
Pentek 7151	256	128–1,024	200	105	64	4.7	0.04	6
Pentek 7152	32	16–8,192	200	105	8	38.3	0.25	44
Pentek 7153	4	2–256	200	120	1	206.2	1.25	29
Pentek 7153	2	2–65,536	200	120	1	612.5	2.5	57

Note [1]: Area per Channel = IC area ÷ number of channels.

Note [2]: GC4016 Power per Channel = Total IC power ÷ number of channels, IP Core Power per Channel = (FPGA power with IP core – FPGA power without IP core) ÷ number of channels.

Note [3]: GC4016 Cost per Channel = cost of IC ÷ number of channels; IP core Cost per Channel = cost of FPGA resources used ÷ number of channels.

Table 1. Performance Characteristics of ASIC and FPGA IP DDC Cores.

Features and Benefits of FPGA-Based DDCs

System Level Savings

Let's now take a look at a complete receiver system. One common application is GSM 2G, a high channel count, low bandwidth system. An E-GMS receiver requires 174 channels spaced 200 kHz apart. Just three or four years ago, a viable solution would have used the TI/Graychip 4-channel GC4016 ASIC-based DDCs. A common board form factor for these types of application is PMC, such as the Pentek Model 7131. One PMC can house two 100MHz A/Ds and four GC4016s and all of the required interface and support circuitry. For a 174-channel system this would require 11 Model 7131's. By comparison, an IP DDC with 174 channels and similar performance to the 4016 can fit in a single Virtex-5 XC5VSX95T FPGA that can be housed on a single PMC, along with 2 channels of 200MHz A/Ds and all support circuitry such as the Pentek Model 7151. A visual comparison of these two solutions is shown in Figure 3.

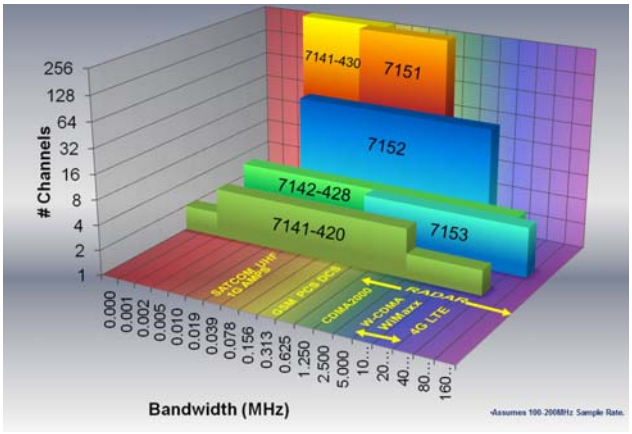


Figure 2. Optimized Core Comparison.

Figure 3. Visual Comparison of the Systems.

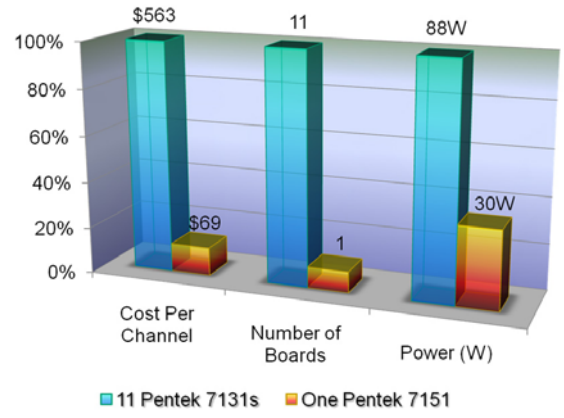


Figure 4. Cost, Board Count and Power Comparison.

Comparing FPGAs and ASICs

FPGAs continue to offer new possibilities and performance when addressing processing tasks like digital downconversion. With each new generation of higher performance FPGAs, processing precision continues to increase. This enables IP-based DDCs to outperform their ASIC-based cousins with specifications like better SFDR.

As shown in Figure 4, it's easy to understand how packing many channels of DDCs into one or two FPGAs can reduce the board count, power requirements and cost over a solution that requires 30 or 40 individual ASIC DDC chips. Additionally, FPGA solutions are extremely flexible since they can support vastly different signals with the simple loading of a different IP core while using the same hardware platform.

FPGA solutions are not a perfect match for all requirements. They show the greatest advantages in systems with high channel densities and, typically, narrower bandwidths. In systems with just one or two channels and bandwidths in the range of 100 MHz or greater, the higher cost of the FPGAs needed can quickly exceed the cost of designing the system with a single multi-channel DDC ASIC. Again, while cost, size and power are important factors in designing a receiver system, ultimately the technical requirements may require the choice of an ASIC or FPGA solution. ❑

Credits

This article is based on the paper *Digital-Down Converter Implementation, FPGAs Offer New Possibilities* by Richard Kuenzler richk@pentek.com and Robert Scandurra bob@pentek.com both of Pentek, Inc. The paper appeared in the September 2008 issue of *Military Embedded Systems*.

Product Focus

Model 7152

32-Channel Digital Downconverter with four 200 MHz, 16-bit A/Ds - PMC

General Information

Model 7152 is a 4-channel, high-speed software radio module designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds supported by a high-performance 32-channel installed DDC (digital downconverter) IP core and interfaces ideally matched to the requirements of real-time software radio and radar systems.

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four T I ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing operations.

DDC Input Selection and Tuning

The Model 7152 employs an advanced FPGA-based digital downconverter engine consisting of four identical 8-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. Many different configurations can be achieved including one A/D driving all 32 DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the 32 DDCs has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sample rate.

Model 7152 is also available in PCI, and CompactPCI formats.

ReadyFlow Board Support Package

Features

- 32 DDC channels in four banks of eight channels each
- Independent tuning for all channels
- Decimation from 16 to 8192
- Bandwidths from 20 kHz to 10 MHz
- Common decimation factor within each bank with different decimation factors between banks
- User-programmable 18-bit FIR filter coefficients
- Default filters with 0.2 dB ripple and 100 dB rejection
- Power meters and threshold detectors
- Clock/sync bus for multimodule synchronization

Decimation and Filtering

All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled with each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Power Meters, Threshold Detectors

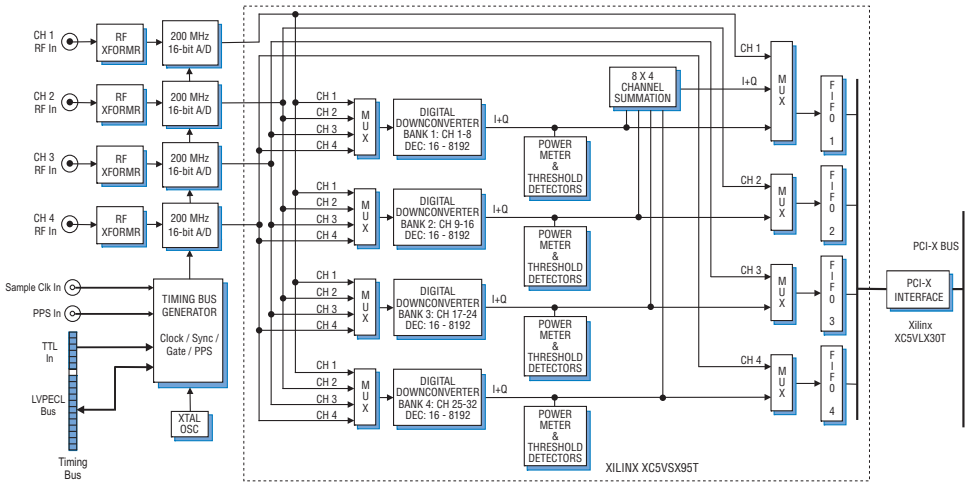
The 7152 features 32 power meters that continuously measure the individual average power output of each of the 32 DDC channels. The time constant of the averaging interval for each meter is programmable up to 16K samples. In addition, 32 threshold detectors automatically send an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold.

Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data.

Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings.

For more information and price quotation on the Model 7152, go to: pentek.com/go/pipe7152. ❑



Product Focus

Model 7153

2- or 4-Channel Digital Downconverter with four 200 MHz, 16-bit A/Ds - PMC/XMC

Model 7153 is also available in PCI, and CompactPCI formats.

ReadyFlow Board Support Package

Features

- 2 or 4 DDC channels
- Four 200 MHz, 16-bit A/Ds
- Independent 32-bit DDC tuning for all channels
- DDC decimation range from 2 to 256 or from 2 to 65536
- Independent decimation factors for each channel
- User-programmable 18-bit FIR filter coefficients
- Default filters with 0.2 dB ripple and 100 dB rejection
- Clock/sync bus for multimodule synchronization

General Information

Model 7153 is a 4-channel high-speed software radio module designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds supported by a high-performance 4-channel installed DDC (digital downconverter) IP core and interfaces ideally matched to the requirements of real-time software radio and radar systems.

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling to four TI ADS5485 200 MHz, 16-bit A/Ds converters. The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing operations.

DDC Input Selection and Tuning

The Model 7153 employs an advanced FPGA-based digital downconverter engine consisting of two or four DDC channels. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC channel. Many different configurations can be achieved including one A/D driving all four DDC channels and each of the four A/Ds driving its own DDC bank.

Decimation and Filtering

Each of the four DDC channels can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. The DDC core can be configured in four-channel mode with each channel offering decimations between 2 and 256; or in two-channel mode with each channel having a decimation range of 2 to 65536, for applications that require a wider range of decimation.

The decimating filter for each DDC channel accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N.

Power Meters, Summation Block

Each channel contains a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 128K samples. The power meters present average power measurements for each channel in easy-to-read registers.

In addition, each channel includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four output channels. The summed output is directed to the Channel 1 FIFO for reading over the PCI-X Bus. For larger systems, multiple 7153s can be chained together via a built-in Xilinx Aurora interface through the P15 XMC connector. This allows summation across channels on multiple boards, ideal for beamforming applications.

For more information and price quotation on the Model 7153 , go to: pentek.com/go/pipe7153. ❑