Learn how to Speed System Development and Optimize Algorithms for COTS Hardware using High-Level FPGA Software Development Tools...

Enpower your software and systems engineers with what they need to know about compatible FPGA design and development resources to port complex algorithms to new FPGA-based reconfigurable COTS hardware platforms for Software Radio, Radar, Imaging, Signal Intelligence and related high-performance real-time signal processing applications.

*O*ur FREE Pentek & Celoxica Joint Technical Seminar will be held on...

**Tuesday, June 15, 2004**
8:30 a.m. until 12:00 p.m.
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**FREE** Technical Seminar:

Fast Track Strategies for Developing and Deploying FPGA-based Systems... Keep up with the latest!

# PENTEK

## FREE SEMINAR

Pentek & Celoxica Joint Technical FPGA Seminar...

# Fast Track Strategies for Developing and Deploying FPGA-based Systems

## What you will learn:

- Why FPGAs are revolutionizing embedded computing

- Tips for optimizing algorithms while shortening development time

- How to reuse custom code as new FPGAs are announced

- How to add your own algorithms to standard, reconfigurable FPGA-based hardware

- How to use off–the-shelf FPGA design tools to implement complex DSP applications

- How to generate RTL and implement hardware directly from the system specification (written in C) — C to EDIF path or C to RTL path

- How to architect complex hardware systems from off-the-shelf COTS hardware

- Effective strategies for upgradeability, spiral development and technology refresh

- How to integrate new industry standard buses and serial switched fabrics into the design mix

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## Seminar Agenda:

(Continental Breakfast from 8:30 a.m. - 9:00 a.m.)

### Introduction:

- Industry Trends in FPGAs and COTS hardware (PCI. PMC, VME, & cPCI)

- Celoxica overview
    - Product details
    - Handel-C
    - IP cores
    - Software development JPEG 2000 image compression example.

- Pentek Overview
    - FPGA system products and high-speed I/O
    - GateFlow FPGA Design Resources
    - GateFlow IP Cores
    - Preview of new Switched Serial Fabric Standards: VXS and XMC

### Application discussion and typical hardware configurations:

- Software defined radio – multi channel synchronous acquisition and real-time signal processing optimized by incorporating FPGAs

- Radar and sonar data acquisition and recording

- Imaging – back scatter application

- Signal intelligence and real-time communications signal processing, recording and display

### Q&A and System Demos:

- Celoxica JPEG 2000 Image Compression
- Pentek FPGA-based Recording Platform

www.pentek.com
www.celoxica.com

## New Product Updates and System Solutions:

RTS 2501 System:
Real-Time Signal Processor and Recorder Development Platform

GateFlow® FPGA Design Kit:
Design your own FPGA application with the aid of Pentek's FPGA Design Kit

GateFlow FFT IP Core:
FFT operates at 20x faster than C6000 DSPs!

GateFlow Wideband Digital Receiver IP Cores:
Fastest wideband receiver available, matches A/D speeds up to 296 MHz!

GateFlow Pulse Compression IP Core with Block Floating-Point Precision

PMC/VIM® I/O Carrier MPC7457 VME processor with on-board Fibre Channel and Gigabit Ethernet (Model 4205)

16-Channel Digital Receiver with A/D and FPGA PCI and PMC Board (Models 7631/7131)

210 MHz 12-bit A/D with Dual Virtex-II Pro FPGAs (Model 6821)

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