

## Field Programmable Gate Arrays (FPGAs) for Software Radio

In the last decade, ASICs (application specific ICs) and DSPs have been deployed to handle nearly all the signal processing functions associated with radio communications. Even though field-programmable gate arrays have been around for decades, the latest generation of FPGAs is so powerful that it is now displacing both ASICs and DSPs in the latest software radio applications. Furthermore, a new class of design tools opens up FPGAs to both hardware and software engineers. Debugging these new devices has been greatly simplified by excellent modeling and analysis tools.

*"With Moore's law at work, these FPGA devices sport incredibly small silicon geometries capable of operating at very low core voltages and very high clock speeds.*

*Most of these new devices take advantage of ball grid array packaging to deliver thousands of I/O pins while keeping the footprint very small."*

Perhaps the most exciting new twist in design tools is the growing libraries of IP (intellectual property) cores available from FPGA vendors, and a whole new industry of third party companies that offer IP cores for specific application areas.

### Software Radio Functions

Figure 1 shows a typical wireless communication software radio system with various signal processing tasks identified. Usually, the digital downconverter or digital receiver section is handled in a dedicated ASIC device consisting of three major blocks: the mixer, the local oscillator and the filter.

The local oscillator, or NCO, consists of a phase accumulator, which is just a register and an adder available as stan-

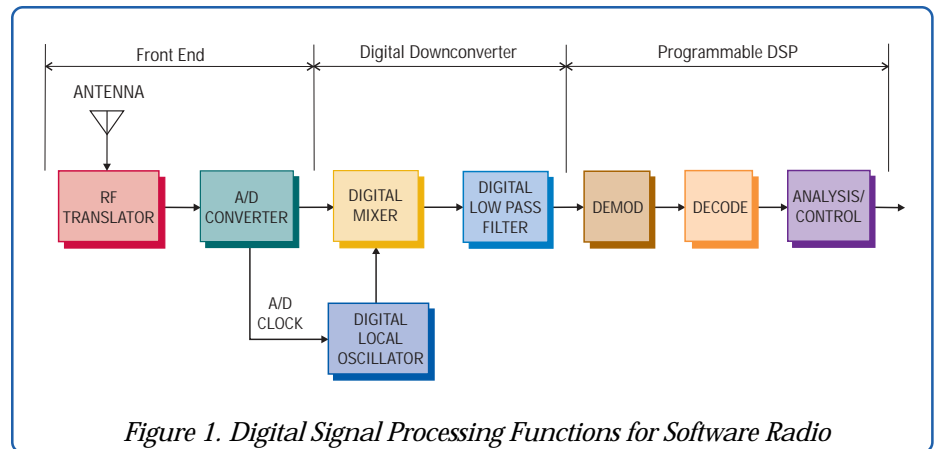


Figure 1. Digital Signal Processing Functions for Software Radio

dard library blocks for virtually all FPGAs. The phase value in the accumulator drives a sine/cosine lookup table which can be implemented as a simple ROM (read-only-memory). The mixer is nothing more than a pair of digital multipliers, now available as dedicated hardware resources in the latest FPGAs.

Programmable DSPs are often used to implement some common demodulation, decoding and analysis functions. However, FPGA vendors and third parties now offer a good selection of IP libraries to handle Viterbi, Reed-Solomon, convolutional and trellis decoders, data encryption standard engines, and various noisy channel models.

Both FFT and discrete cosine transform cores are also available with several different block lengths. Several vendors are offering scalable FFT engines ranging in size from 16 to 1024 points and higher using complex radix 4 algorithms. Since the FFT operates on blocks of data, the block memory RAM available with the newer FPGA devices allows some design tradeoffs. You can save memory by doing an in-place FFT with a single block, or move up to a swinging buffer arrangement to provide continuous real-time calculations.

To help with control functions, a long list of IP cores is available for popular processors. The benefit here is that by using a well-supported core processor, one can take advantage of existing code and the software development tools already in place for these engines.

For speech and video signals, a wide range of IP cores including ADPCM, J-PEG and color space converters is available. The same is true for the decimating low pass filter which usually consists of several CIC filter stages followed by a FIR filter. If some or all of these signal processing functions are handled by the FPGA, the programmable DSP can then concentrate on the control and analysis functions, much more appropriate for its capabilities.

### Digital Receiver ASICs vs. FPGAs

Although digital receiver functions can be implemented within the FPGA, it can draw more power and cost much more per channel than an ASIC, depending on many factors like sampling frequency, filter characteristics, and signal-to-noise requirements.

Usually, the ASIC digital receiver has been designed with a full set of standard operating modes and features and has ➤

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[Continued from page 1] been more thoroughly tested and characterized than a custom combination of IP core building blocks available for FPGAs. This gap will obviously shrink as the cores become more complete. Since the ASIC hardware is optimized for dedicated functions, the latest ASIC devices are usually the better choice for extremely high-performance receiver applications.

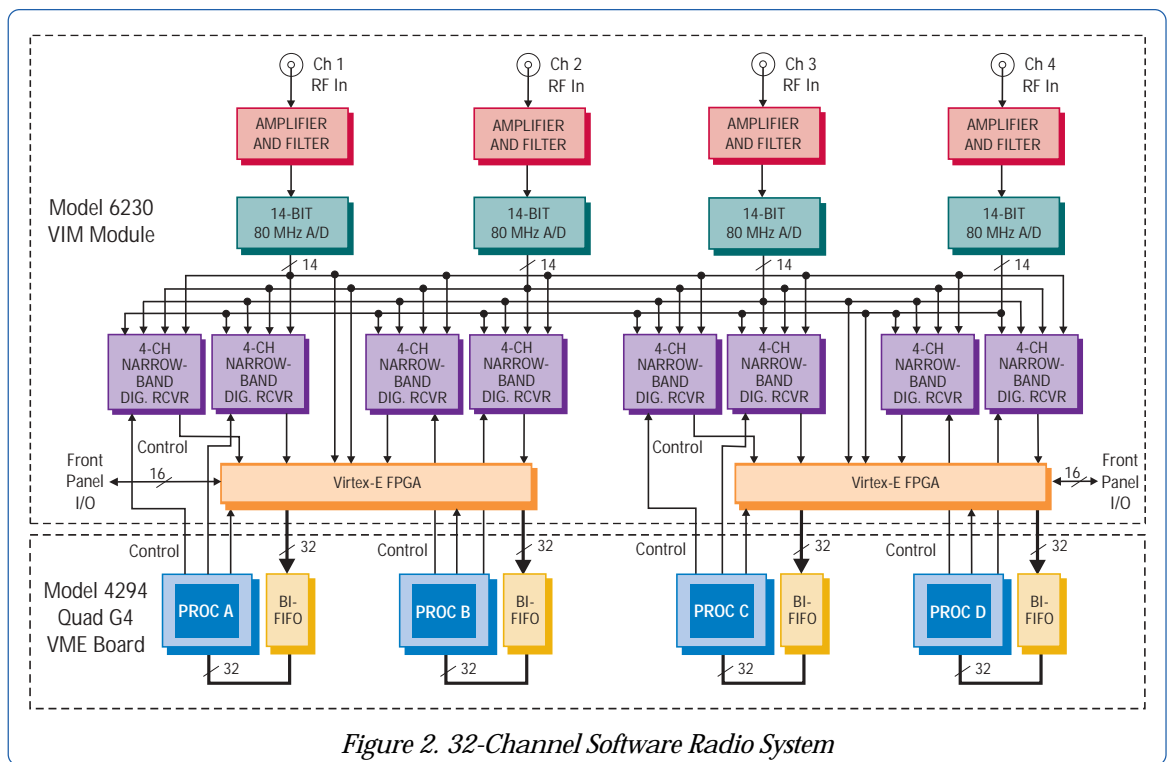


Figure 2. 32-Channel Software Radio System

*“FPGAs are successfully taking up many of the roles formerly played by DSPs and ASICs. One of the major benefits of the IP core concept is that, like high-level languages, these cores can migrate to the next generation devices. This means that the wealth of core functions can accumulate and diversify, eliminating the need to start over again for each new family.*

*More information on devices and cores is on the internet. New announcements are appearing daily and a good springboard for information is the third party section of FPGA vendors’ web sites. Certain third parties are true experts in niche application areas and many of them offer consulting or custom design services as well.”*

However, if you can’t buy a standard digital receiver ASIC with just the right phase and frequency characteristics, the flexibility of the FPGA might get the job done. Also, for proof-of-concept

systems or when time-to-market is critical, FPGAs are often the right choice.

In other applications, where the required signal-to-noise ratios, filter skirts, or frequency templates are beyond the complexity of the standard filter inside a commercial ASIC, the flexibility of IP core filter designs for FPGAs can provide just about any characteristic.

### DSPs vs. FPGAs

While FPGAs can handle many of the tasks traditionally performed on a programmable DSP chip, there are several factors worth considering. For example, even though today’s FPGAs have quite a bit of on-board RAM, it’s still a far cry from the large external SDRAMs normally surrounding a DSP chip. In spite of all the best design tools and simulators, DSP code (like any software) always seems to need more memory sooner or later. Newer FPGAs are now capable of embedding SDRAM controller cores to help alleviate this shortcoming.

While FPGA code can be reconfigured for new modes of operation and

feature enhancements, it’s usually much easier to make the more significant changes on a programmable DSP instead. Sometimes, a very small change can have a profound impact on the gate and logic cell topology.

### System Example

Figure 2 shows a 32-channel digital receiver system suitable for a wide range of applications such as signal intelligence, direction finding, and signal tracking receivers. It consists of a Pentek Model 6230 VIM-4 mezzanine module attached to a Model 4294 Quad G4 PowerPC VIM processor board at the bottom.

The receiver module has four 14-bit 80 MHz A/D converters for digitizing IF or HF analog inputs entering through front panel SMA connectors. All four A/Ds feed a bank of eight quad digital downconverter ASICs with four channels of local oscillator, mixer and filter in each chip.

On board are two Xilinx Virtex-E FPGAs, each receiving the sixteen baseband signals from the four quad

## 32-Channel Digital Receiver VIM-4 Module With FPGAs and FPDP Inputs

[From page 4]  
ing the sample clock out to a front panel cable bus using LVDS differential signaling. Multiple slaves can then be clocked synchronously with the master. Additional sync lines on the bus allow synchronization of the local oscillator

phase, frequency switching, decimating filter phase, and FIFO data collection on multiple 6232's.

### FPGAs

The 32 receiver outputs are delivered to two Xilinx Virtex-E Series

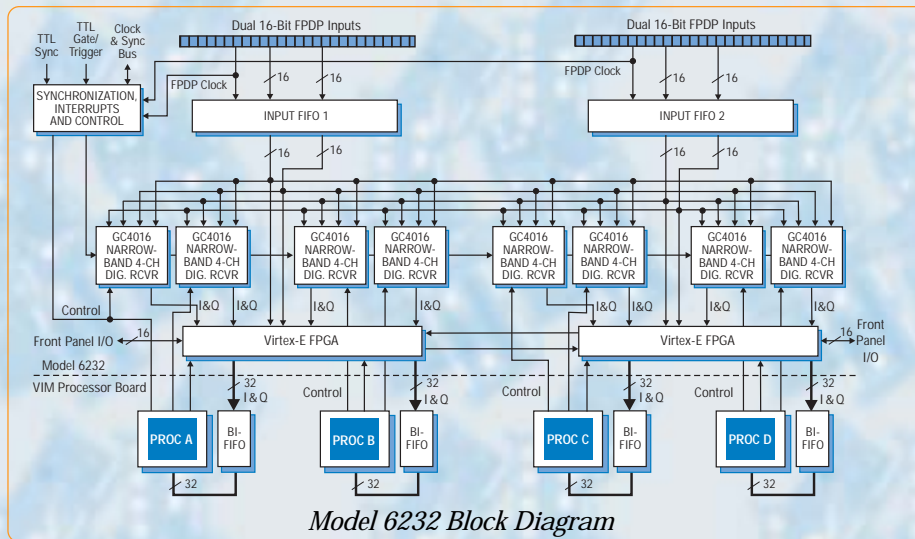
XCV300E FPGAs (field programmable gate arrays) which perform various modes of data packing, formatting and channel selection. Model XCV600E FPGAs are also optionally available.

Optionally available design kits allow the FPGAs to be configured by the user for implementing custom preprocessing functions such as convolution, framing, pattern recognition and decompression.

### VIM Processor Interface

The FPGA outputs are connected directly through the VIM mezzanine interface to the 32-bit synchronous FIFO on the VIM baseboard where it is buffered for efficient block transfers into the processor. The processor can control the programmable registers on its associated GC4016's as well as control and initiate sync bus functions.

For more information, visit our website at <http://www.pentek.com/products/detail.cfm?model=6232> □



receiver chips. The FPGAs are used to handle data formatting and channel selection for delivery through the VIM interface to the 32-bit mezzanine FIFOs on the processor board. Since the receiver signals flow through the FPGAs, they can also be used to perform demodulation and decoding functions to offload these tasks from the DSP.

All four A/Ds are connected to all eight quad receiver chips. Inside the front end of each receiver chip is a programmable crossbar switch that allows each of the four narrowband channels inside to independently select any one of the four A/D inputs.

This means all 32 receiver channels on board can independently select which A/D or antenna they are looking at. This provides a very dynamic antenna-to-channel assignment scheme for systems that need to adapt to changing traffic patterns.

The digital outputs of two A/D converters are delivered directly into each FPGA. This allows wideband A/D data to stream directly through the FPGA to the DSP since the high bandwidth of

the VIM interface supports clock rates up to 100 MHz.

Even more important, it also allows the FPGA to handle signal processing algorithms on the raw A/D data before it goes to the DSP, again, to offload some of its processing tasks. After handling the factory standard functions of data formatting and control, nearly 70 percent of these resources is still available for custom applications.

The factory default code takes care of all the basic functions for most applications, including selection of channels for delivery to the DSP board, selection of real or complex data modes, selection of receiver data or raw A/D data, and selection of data packing modes. For custom signal processing tasks, the optional design kit for each product includes the VHDL source code for all these standard factory default modes.

Users can extend the factory code by adding their own algorithms at appropriate points in the signal flow path. FPGA algorithms can be developed and simulated by drawing on the wealth of IP cores and design tools available

for these devices. Once compiled, the custom code can be downloaded through utility loaders into a non-volatile user memory on the board. □

## Upcoming Trade Shows

Here's a quick synopsis of the trade shows Pentek will be exhibiting during the first four months of 2002. Please come visit with us, so we can discuss your signal processing application.

Date	Location	Show Name
Jan. 21	Long Beach, CA	Bus & Board
Jan. 29	Jan Jose, CA	Real Time
Jan. 31	Portland, OR	Real Time
Feb. 12	Phoenix, AZ	Real time
Feb. 14	Albuquerque, NM	Real Time
Mar. 4	Col. Springs, CO	Real time
Mar. 5	Denver, CO	Real Time
Mar. 7	Salt Lake City	Real Time
Apr. 2	Melbourne, FL	Real Time
Apr. 4	Huntsville, AL	Real Time
Apr. 16	Minneapolis, MN	Real Time
Apr. 30	Boston, MA	Real Time

# Product Focus

## 32-Channel Receiver With FPGAs and FPDP Inputs VIM-4 Narrowband Digital Receiver Module Has Two Virtex-E FPGAs

### Model 6232



*Model 6232 won ECN magazine's Best of the Web 2001 Award.*



*Model 6232 is supported by Pentek's ReadyFlow Board Support Libraries for easier and faster system development.*

Model 6232 is a 32-channel narrow-band digital receiver VIM-4 module. It attaches to VIM-compatible boards and connects directly to all four processors.

#### Front End

The Model 6232 accepts four 16-bit digital inputs on two front panel FPDP connectors supporting data rates up to 40 MHz (optional FPDP II compatibility – to 80 MHz – is planned for future availability). Data from each 16-bit input flows into a FIFO to allow synchronization, and is in turn transferred to the digital receiver section. Data from any of the four inputs can be directed to any of the 32 receiver channels or directly to the FPGAs.

Each FPDP connector is clocked individually. Clock information is sent to a controller for data clocking and sync.

#### Digital Receivers

The 6232 includes eight Graychip GC4016 quad narrowband digital receiver chips. The maximum input sampling rate for the GC4016 is 80 MHz. Each device includes four independently tuned receiver channels capable of center frequency tuning from DC to 20 MHz, and with output bandwidths ranging from 2 kHz to 1 MHz (for 40 MHz sample clock).

Each GC4016 accepts up to three 16-bit or four 14-bit parallel inputs from the input FIFOs. Internal crossbar switches allow all 32 receiver channels on the board to select any of the four A/D inputs for flexible switching.

#### Synchronization

The front panel clock and sync bus allow one 6232 to act as a master, driv-



We are pleased to announce that Pentek's Model 4294 Quad G4 PowerPC processor VME board was selected by EDN magazine as one of its Hot 100 Products of 2001! Go to [www.pentek.com/powerpc](http://www.pentek.com/powerpc) for more information.



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