The Pentek Pipeline
A quarterly publication for engineering system design and applications.

Fall 2001 • Vol. 10, No. 3

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Pentek DSPs Keep the ELETTRA Photon Beam Stable and Bright

ELETTRA is a third-generation synchrotron radiation facility in Trieste, Italy. The facility provides the scientific community with photons in the range of a few electron volts (eV) to several tens of thousands (keV), the latter corresponding to the spectral domain of soft X-rays. The main characteristics of the synchrotron radiation are very high brightness, polarization and wide range of tunability in wavelength.

Figure 1 is an aerial photograph of the facility. The light source is composed of three parts: a linear accelerator (commonly known as a linac), a transfer line and the storage ring. The storage ring is filled once a day by the linac with 0.9 GeV electrons whose energy is eventually increased up to 2 – 2.4 GeV.

Figure 1. The ELETTRA facility in Trieste, Italy (Courtesy of ELETTRA).

Synchrotron radiation is produced when electrons traveling at relativistic speeds are deflected in magnetic fields. The brightness of the photon beam is derived from the small transverse size and divergence of the electron beam, and is called emittance.

Low emittance, stability, reproducibility and long lifetime of the stored beam are the main requirements for the light source. These properties are a function of the beam environment, e.g. the magnetic field lattice, the accelerating electric fields and the quality of vacuum in the vacuum chamber.

Since the beam is guided in the storage ring by vertical and horizontal focusing magnets, their characteristics are of utmost importance. Magnet misalignment distorts the orbit and induces spurious dispersion, which leads to increased emittance and reduction in photon brightness.

As disturbances have different time scales ranging from milliseconds to months, different techniques are used for their suppression and control. Although much is done to passively control instabilities, active feedback systems working at different frequencies and with different bandwidths are needed. Given the small size of the beam (typically tens of microns), stabilizing it requires outstanding performance in position measurement and correction.

System Overview

The electron beam stored in a synchrotron light source is not a continuous beam. It has a "bunched" structure produced by the effect of one or more RF cavities installed in the ring and used to replenish the energy lost by the electrons as electromagnetic radiation on each turn. The reason for this bunch structure is because only electrons arriving at the right time will be accelerated, while the rest are lost. At ELETTRA, the RF frequency of the four cavities is 500 MHz, so the electron bunches are spaced 2 nsec apart.

As currents in the ring are increased, the very high electromagnetic field associated with each bunch interacts with the surrounding vacuum chamber and can start resonating, in one or more storage ring positions, until the next bunch arrives. As a result, the bunches are no longer independent, but they become coupled to each other by the action of their respective electromagnetic fields. The result is that bunches start oscillating at a characteristic frequency, the betatron frequency (in the order of a few hundreds of kHz), but with different phase relationships among them resulting in different "modes". There are as many normal modes as there are bunches. In the case of ELETTRA, there are 432.

Such coupled-bunch instabilities can be cured by the use of active feedback systems. The approach used at ELETTRA involves a digital feedback system that samples the bunch positions in the storage ring and applies corrections computed by digital signal processors. As shown in Figure 2 on page 2, the system includes a 2-axis "Beam Position Monitor" (BPM) and a position corrector, appropriately called a "Kicker". One BPM is used to produce the vertical and horizontal ➤

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position error signals, while two stripline kickers are used for correcting in the two planes.

The wideband signals are demodulated by the RF front end to produce a 0–250 MHz baseband signal that represents the position error of the bunches as they pass through the BPM at a frequency of 500 MHz. The output analog signal is sampled by a fast 500 MHz A/D converter and passed onto a bank of DSPs that calculate the required correction. The correction is then converted into analog form by a 500 MHz D/A converter. The analog signal represents the correction that has to be applied to the bunches as they pass through the kicker. A RF power amplifier supplies the necessary power to drive the kicker.

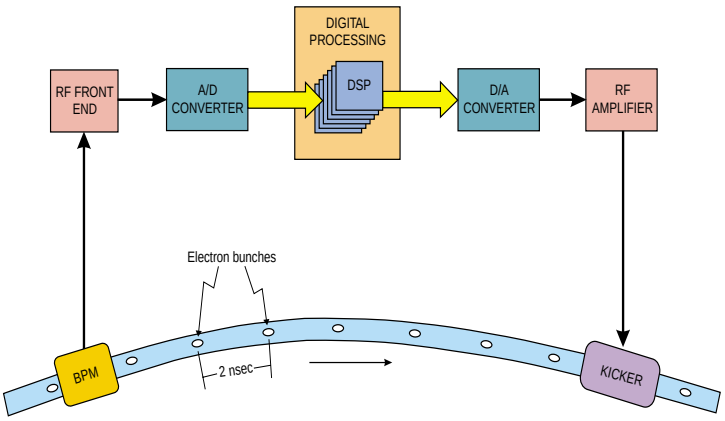

Figure 2. Feedback System Block Diagram.

Signal Processing

The ELETTRA Transverse Multibunch Feedback consists of a wideband bunch-by-bunch system where the position errors of the 432 bunches, separated by 2 nsec of beam travel time, are individually corrected. After demodulating the wideband signal from the BPM, the baseband x and y signals are sampled by 8-bit 500 MHz A/D converters. One converter is used for the vertical signal and another one for the horizontal. We will address the vertical position signal processing first.

As shown in Figure 3, the 500 Mbyte/sec data flux is first demultiplexed into six 32-bit FPDP (Front Panel Data Port) channels. The data from each channel is then sent through a custom VIM-4 mezzanine module designed by ELETTRA to meet the needs of this project. It provides a FPDP interface with the demultiplexer to distribute the A/D data to the four DSPs of the Pentek Quad ’C6201 board. The data coming from one FPDP channel, which corresponds to 72 bunches, is passed to one DSP for online diagnostics and signal analysis. Concurrently, the data is split evenly over the remaining three DSPs, each of which executes the feedback algorithm on its respective 24 bunches. Thus, each DSP is responsible for processing the samples of a given group of bunches all the time.

To process all 432 bunches, six Model 4290’s containing 24 ’C6201’s are used. The FPDP input interface receives 32-bit words and writes them to the BI-FIFO of the DSP to which they are specifically assigned for processing. At the same time, the VIM-4 mezzanine reads the BI-FIFO which contains the calculated data words and sends them to the FPDP output interface. The FPDP interfaces act as bidirectional programmable switches for each incoming and outgoing word and the switching rules are downloaded in a table at the beginning of system initialization.

The output data from the six custom FPDP mezzanines are multiplexed by the D/A board and converted to analog form by the 8-bit 500 MHz D/A converter. The entire process is synchronized by the timing electronics.

All the electronics required to stabilize the beam in the vertical direction are housed in one VME cage in the service area. One additional VME cage with identical electronics is used for the horizontal direction.

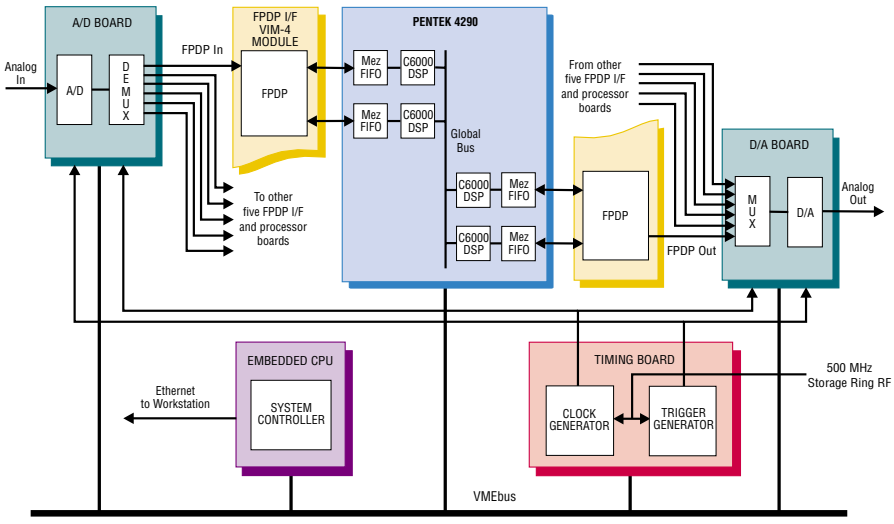

Figure 3. Signal processing block diagram.

Critical Issues

The ’C6201 is a fixed-point DSP clocked at 200 MHz (5 nsec instruction cycle). Its VLIW architecture allows it to execute up to 8 instructions per clock cycle. The requirement here is to execute all the necessary operations ➤

Configurable Logic FPGA VIM-2 Module with FPDP I/O

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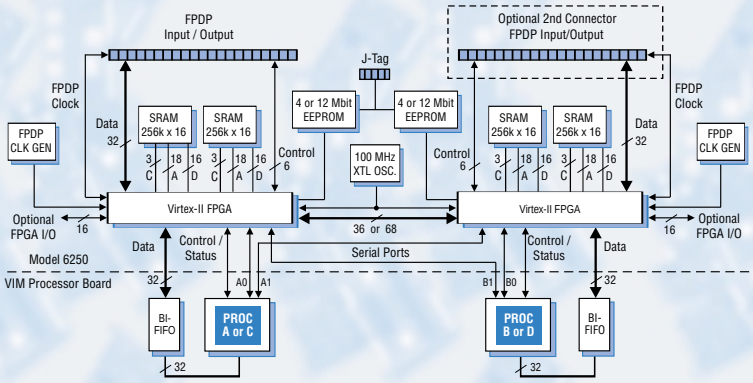
connected to the FPGA with separate address and data buses so they can be used independently. The SRAMS can be used for storing data without consuming internal FPGA logic cells to implement RAM.

FPDP Interfaces

One front panel FPDP interface is provided in the standard configuration with a second FPDP available as an option. These interfaces are bidirectional and designed to be compatible with future FPDP-II peripherals.



Model 6250 Block Diagram

Two Model 6250's may be attached to a VIM-compatible processor board to provide twice the capability in one slot. Alternately, the 6250 may be combined with a different VIM-2 module for additional I/O functionality.

FPGA Programming

An optional FPGA design kit to be used in conjunction with the Xilinx Foundation development tool suite is provided. It includes VHDL source files for the VIM interface and control registers for the clock functions. Templates for implementing custom signal processing blocks are included with detailed instructions. FPGA code may be downloaded from the processor node or permanently stored in non-volatile memory.

Third-party sources for IP signal processing core libraries compatible with the Virtex-II support a wide range of popular algorithms and functions. These include FFTs, FIR filters, compression and decompression algorithms, software radio blocks, decryption, telemetry functions, decoders, and convolution.

For more information, visit our website at **http://www.pentek.com/products/detail.cfm?model=6250** ❑

in one beam revolution, or 864 nsec (2nsec x 432 bunches). With a highly optimized code written in assembly language, the time needed to execute the required code of a 5-tap FIR filter, which is used as the feedback element on the 432 bunches, is 600 nsec which is shorter than the beam revolution time.

Another critical issue is the time required for data transfers between the DSP and its BI-FIFO. To minimize the time data stays on the board, thorough use of the Pentek BI-FIFOs, interrupts and DMAs allows very efficient data transfer without interfering with the algorithm execution.

The feedback system relies on very strict timing. The A/D converter must sample the analog signal synchronously to the bunch crossing at the BPM and the D/A converter must generate the analog correction signal in phase with the same bunch passing through the kicker. In addition, the start A/D and D/A triggers must start the conversions in a deterministic and repeatable way with respect to the bunch structure in order to let every DSP work with a known group of bunches.

Results

Figure 4 consists of two synchrotron beam profile images: the one on the left is with the feedback loop open, while the one on the right was taken with only the vertical feedback loop closed. The photographs show how effective the control is at improving beam stability.

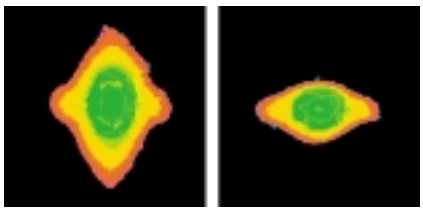


Figure 4. Synchrotron beam profiles: left, without feedback; right, with vertical axis (only) feedback stabilization. (Courtesy of ELETTRA)

ELETTRA and APS

In the Summer of 1997 issue of The Pentek Pipeline, we featured the Advanced Photon Source (APS) at Argonne National Laboratory. Both APS and ELETTRA are synchrotron light sources of the so-called "third generation". APS is a physically larger machine with a circumference of 1104 meters and higher energy of 7 GeV. It is optimized for the production of hard X-ray radiation. With a circumference of 259 meters, ELETTRA is a smaller machine and is optimized for the production of soft X-rays. Both types of X-rays are used in scientific research, depending on the application.

The APS feature article provides more details on the generation and steering of the photon beam but no discussion of the electron bunches. In this article, we concentrated on the multibunch feedback scheme and the signal processing.

The APS feature article is available on Pentek's website at http://www.pentek.com/dspcentral/c40/Articles.cfm

To dig deeper, visit ELETTRA's site at: www.elettra.trieste.it and the Advanced Photon Source site at: www.aps.anl.gov ❑

Product Focus

Model 6250

Configurable Logic FPGA VIM-2 Module with FPDP I/O

Includes two Xilinx Virtex II FPGAs and two FPDP Interfaces

ReadyFlow Board Support Libraries

Model 6250 is supported by Pentek's ReadyFlow Board Support Libraries for easier and faster system development.

Model 6250 is a Configurable Logic FPGA VIM-2 module with FPDP I/O. It features up to two FPDP (Front Panel Data Port) interfaces, and two Xilinx Virtex II FPGAs (field programmable gate arrays).

The Model 6250 supports custom, high-performance signal processing and computing functions for any VIM-compatible processor board.

As a VIM-2 module, Model 6250 connects to two of the four processor nodes, leaving the other two available for a second VIM-2 module to provide additional functions.

FPGA Devices

The Model 6250 may be equipped with one of two FPGA devices in the Xilinx Virtex-II family: Model XC2V-1000, or XC2V-3000.

Each FPGA interfaces directly to all three sections of the associated VIM interface: both serial ports, the 32-bit BI-FIFO parallel port and the control/status port. The BI-FIFO buffers on the processor board allow the processors to move blocks of data efficiently to and from each FPGA.

The two FPGAs are interconnected with up to 68 (XC2V-3000) programmable user I/O lines to support data and control passing between the two devices. An optional connector is available for FPGA front panel I/O.

SRAM

Each FPGA is equipped with two 256k x 16 SRAMs. Each SRAM is ➤

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