The Pentek Pipeline
A quarterly publication for engineering system design and applications.

Spring 2001 • Vol. 10, No. 1

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AT&T Labs-Research Designs a Broadband Radio Link for Internet Access

We covered some of the work at AT&T Labs-Research in Pipelines Vol. 8, No. 1 and Vol. 8, No. 2 (Spring and Summer 1999). Both articles discussed work related to improving cellular communications. This article involves one of today's hot topics, broadband Internet access. We'll cover the implementation of the first phase of an experimental radio link for high-speed access to the Internet. The first prototype delivers 384 kbits/sec, an order of magnitude faster than currently available in a cellular system, and paves the way for a further one to two order of magnitude increase in data rates.

The interest in wireless high-speed access to wide area networks has grown considerably in recent years. The interest is fueled by significant improvements, such as cable modems and DSL for wideband access to the worldwide web, the widespread availability and acceptance of mobile computing devices, such as notebook computers and PDAs, and the global deployment of wireless voice communications systems. Wireless broadband Internet access is now beginning to generate interest in those who cannot get broadband access to the web via cable modem or DSL or for users who need broadband access while on the move. Unfortunately, today's harsh radio environment creates challenges when trying to provide high-speed access, especially for the high mobility conditions found in cellular networks.

In this article, we'll discuss the implementation of a wireless system proposed for use as the downlink for high-speed (384 kbits/sec and faster) Internet access. The experimental system employs Orthogonal Frequency Division Multiplexing (OFDM) and real-time implementation.

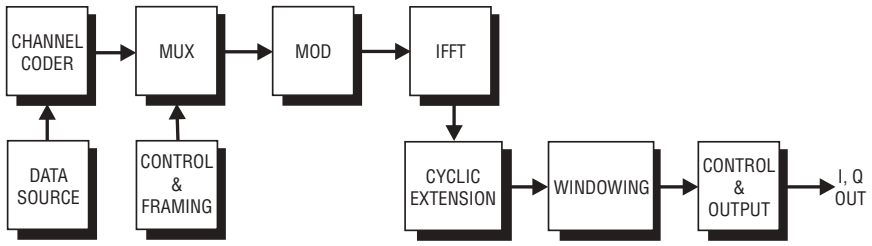

Figure 1. OFDM Transmitter

OFDM Background

In an OFDM system, a single high-speed bit stream is separated into several low-speed bit streams, with each of the slower bit streams used to modulate one of several carriers. The carriers are generated within a single bandwidth with their frequency spacing chosen to insure orthogonality of the resulting combined waveforms.

You could build an OFDM system by generating a number of sinusoidal carriers and modulating them individually. However, a modern OFDM transmitter is typically implemented by generating a series of complex numbers. Each complex number represents the amplitude and phase of the individual tones.

This series of tones is converted into a time domain waveform through the use of the Inverse Discrete Fourier Transform (IDFT), or to reduce complexity, the Inverse Fast Fourier Transform (IFFT). For practical reasons, the IFFT is usually somewhat larger than the number of tones. Unused tones at the edge of the band are set to zero to eliminate energy outside the desired bandwidth. This approach makes the analog reconstruction and anti-aliasing filters more easily realizable.

The OFDM receiver uses a forward FFT to transform the received waveform back to a set of orthogonal tones, while ignoring the unused tones. The complex numbers that represent the received amplitudes and phases of the tones correspond directly to the modulating carriers, allowing simple demodulation of the received carriers.

The OFDM Transmitter

Figure 1 shows a simplified block diagram of an OFDM transmitter. The output is a complex baseband signal, which is translated to RF by a quadrature modulator. The number of active tones is chosen to provide the desired bandwidth and data rate of the system. In this case, 189 active tones are used and a 256-point IFFT could be used to minimize the signal-processing task. However, the smaller IFFT would have resulted in a baseband signal with a stopband that began at about 1.5 times the highest desired frequency. Because of filter complexity and the need to control group delay distortion, a 512-point IFFT is used. This choice results in a filter with a stopband frequency four times the highest frequency of interest.

The OFDM transmitter imparts additional information to the IFFT samples, referred to as a "cyclic extension": transformed samples are copied from the beginning (and/or end) of the block to the end (and/or beginning) ➤

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of the block. Because of the time-shifting property of the Fourier Transform, delayed copies of the transmitted signal, caused by multipath distortion, do not degrade the received signal as they might for other types of communications systems. Two other segments are added to the IFFT, the guard interval and the windowed section. During the guard interval, the transmitted samples are all set to zero. This ensures that the samples received during a given OFDM block are not contaminated with delayed samples from a previous block, or from a different distant base station. Since the OFDM system is used in packet mode, it is expected that the transmitter will be turned on and off during each signal burst. Windowing of the OFDM samples is used to prevent the radiated signal from causing interference outside its assigned channel due to rapid turn-on and turn-off.

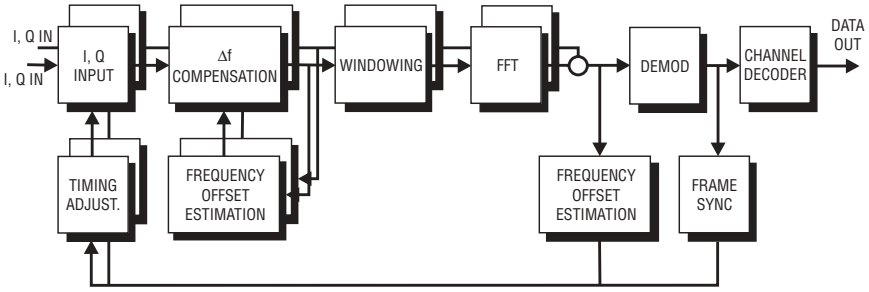


Figure 2. OFDM Receiver

The OFDM Receiver

The OFDM receiver shown in Figure 2, mirrors the operation of the OFDM transmitter. Again, time domain and frequency domain signals are treated as complex. Receiver windowing is used to improve adjacent channel interference and the receiver time samples are converted to the frequency domain by a forward FFT. While the relatively long period of the OFDM waveform makes the system resistant to delay spread, incorrect timing of phase or frequency offset in the received signal will degrade system performance. To prevent this, the amount of timing offset in the received signal is estimated and the phase of the sampling clock is continuously adjusted to drive the offset to zero. Likewise, frequency offset is estimated and is compensated by performing a complex multiplication between the received samples and a complex vector rotating at the estimated offset frequency. Two complete receiver front ends were implemented to provide the advantages of maximum ratio combining (MRC) of antenna diversity.

Signal Processing

The system is implemented using the Pentek 4270 Quad 'C40 DSP processor boards. Multiple DSPs are assigned different functions. As shown in Figure 3, to implement the OFDM receiver, the functions were allocated to the DSPs of two 4270 boards as follows:

- FFT front end processing, including acquiring samples from the Pentek 6109 A/D converter at a 2.166 MHz sample rate, frequency offset compensation, windowing and calculating 512-point complex FFTs is assigned to two of the 'C40s of the first 4270 board, one per receiver channel. These DSPs also calculate estimates of the frequency offset. Each DSP ('C40A and 'C40B), is used to perform these functions for one of the complex IQ channels.
- Demodulator processing including static gain balance between receiver channels and demodulation is assigned to the next DSP, 'C40C.
- The fourth DSP, 'C40D, is responsible for Decoder processing, framing detection and maintaining frame error statistics.
- Signal control processing, including sending gain and frequency control words to the external RF unit, measuring receive signal power levels for gain control, estimating timing offset and sending timing and frequency offset corrections and sample clock instructions are performed by the first DSP, 'C40E of the next 4270 board.
- The next DSP, 'C40F, performs control monitor functions, including real-time user control of receiver parameters and allows real-time display of various signals throughout the receiver.

The entire OFDM receiver is implemented with six DSPs in two Pentek 4270 boards. All interprocessor communications occur via shared global memory access. Transfers take place over the MIX bus and processor synchronization between the two receiver channels is maintained in the software.

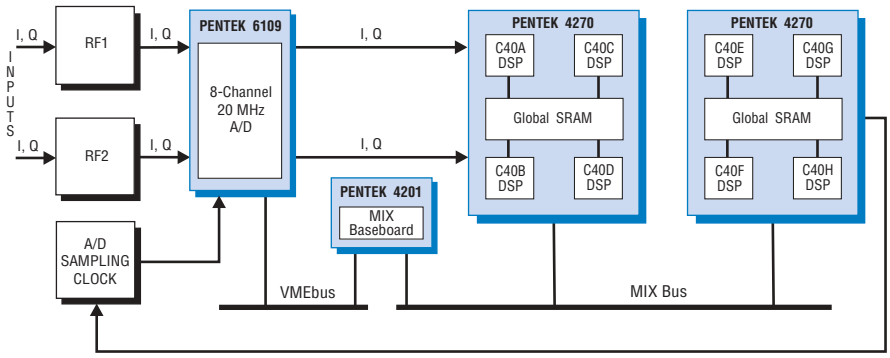
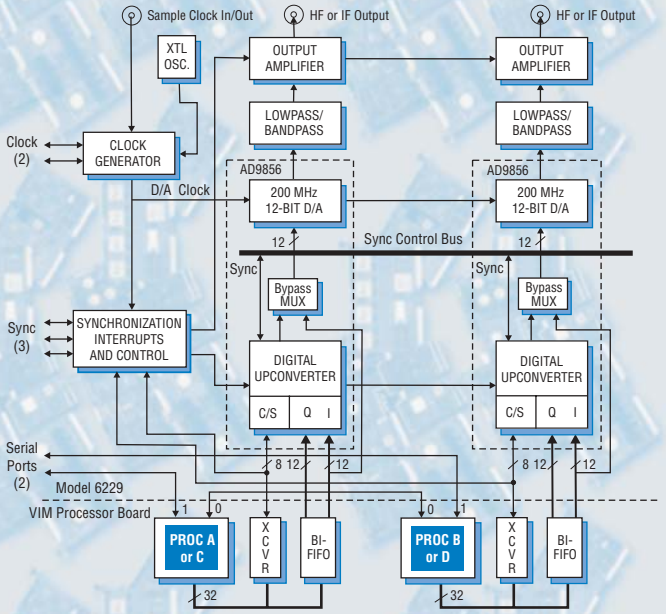


Figure 3. Block Diagram, OFDM Receiver Signal Processing

Dual Digital Upconverter and D/A VIM-2 Module



Model 6229 Block Diagram

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programmed to cover an LO range from DC to 80 MHz.

The translated single sideband signal, sampled at 200 MHz, is fed into an on-chip 12-bit D/A converter, capable of producing analog outputs up to 80 MHz.

An optional inverse sinx/x filter can be inserted in the signal path prior to the D/A to compensate for its zero-order hold frequency response.

Complex baseband samples generated by the baseboard processor are sent into the 6229 through the 32-bit parallel BI-FIFO path. Data may be packed with both I and Q components in a single 32-bit word for more efficient transfers.

For applications requiring a non-translated baseband D/A output, samples from the processor board can be upsampled without frequency translation and sent to the D/A converter.

Pentek's Readyflow™ Board Support Libraries are available for this product.

For more information on the 6229 or any of our VIM products, visit our website at **http://www.pentek.com**. ❑

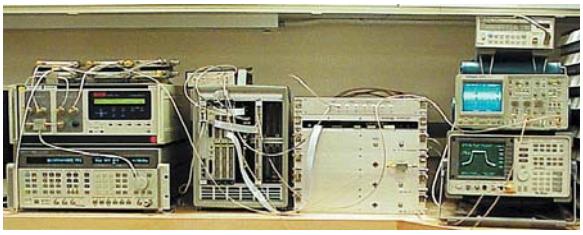

Figure 4. Base Station Prototype (Courtesy of AT&T Labs-Research)

Figure 4 shows the base station prototype. From left to right, the basic blocks of the system are:

- The RF channel simulator which includes a HP synthesizer as a local oscillator and attenuators to set signal levels.
- The DSP signal processing hardware in a VME cage.
- A RF transceiver plus home-designed modules to provide the baseband interface.
- An oscilloscope displaying the OFDM waveform and a spectrum analyzer displaying the RF signal.

What's Next

The OFDM project demonstrated the practical considerations of system design and has yielded results that were in close agreement with theory. The results will be used to guide and validate decisions for the next generation, higher speed system.

The next phase of OFDM investigation focuses on 2-10 Mb/sec high-speed access and builds on the work and results of this project. To attain good performance at reasonable SNRs, antenna diversity and forward error correction coding will be required. It is also expected that interference cancellation, more sophisticated coding, and adaptive modulation techniques will be required. See Pipelines Vol. 8 No. 1 and Vol. 8 No. 2 for more information on these topics.

Future work will involve combining these OFDM techniques with Smart Antenna and Multiple Input Multiple Output (MIMO) experiments that have also been accomplished with Pentek hardware. These techniques hold the promise of mobile data rates up to 40 Mb/sec. ❑

Model 6229 wins Top 20 Product Award

The Pentek 6229 Digital Upconverter was one of 20 products introduced in 2000 that won Wireless Design & Development's Technology Award. The award is given to products that display unique and innovative design and usefulness to the wireless industry.

Back at Pentek's corporate headquarters, the 6229 development and applications team is all smiles accepting the award plaque from Rodger Hosking, Pentek Vice President and cofounder.

"You should all feel very proud of this award which recognizes your contribution to the definition and development of a truly outstanding product," he said. ❑

Product Focus

Model 6229

Dual Digital Upconverter and D/A VIM-2 Module

Wins Wireless Design & Development's Top 20 Product Award

Intended for Pentek's VIM-compatible processor boards, Model 6229 contains two complete channels of interpolation and frequency translation suitable for linking a DSP system to a radio transmitter.

Applications include generation of communication and radar test signals, electronic countermeasures, and implementation of transmit functions for advanced software radio communications systems.

Model 6229 was one of 20 products introduced in 2000 that won Wireless Design & Development's Technology Award during the Wireless/Portable Symposium and Exhibition held in San Jose, CA in February.

Digital Upconverter

The 6229 uses the AD9856 Quadrature Digital Upconverter which includes half-band and CIC interpolation filters, a programmable local oscillator, a complex mixer, and a 12-bit D/A converter.

An on-chip multiplier accepts a reference clock from 5 to 50 MHz and multiplies it to a maximum 200 MHz internal sampling clock.

The reference clock can be driven from a local 50 MHz crystal oscillator or from an external input reference. A front panel ribbon cable allows multiple slave 6229's to be driven from a single designated master 6229.

Complex baseband data samples consisting of 12-bit I+Q pairs are accepted at rates as high as 25 Msamples/sec.

Three halfband interpolation filters upsample the baseband input by 4x or 8x. Additional upsampling is performed by a CIC filter which interpolates by x2 to x63 in steps of 1, providing an overall interpolation range from x8 to x504.

Complex local oscillator samples are generated by a direct digital frequency ➤