New!

# Model 7142-428 Installed Core

# GateFlow Transceiver with Four Multiband DDCs and Interpolation Filter - PMC/XMC

ReadyFlow Board Support Libraries

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## Features

- Complete software radio transceiver solution
- GateFlow Core 428, with four high-performance multiband DDCs and Interpolation Filter, factory-installed
- Improved dynamic range
- Two sets of 18-bit user-programmable FIR filter coefficients
- Decimation range from 2 to 65,536
- Interpolation range from 2 to 32,768

## Ordering Information

| Model | Description |
|---|---|
| 7142-428 | Gateflow Transceiver with four DDCs and Interpolation Filter factory installed - PMC/XMC |

## General Information

Model 7142-428, Digital Transceiver with Multiband DDC Core and Interpolation Filter, is a complete software radio system in a PMC/XMC module. It includes four A/D and one D/A converters capable of bandwidths to 40 MHz and above for connection to HF or IF ports of a communications or radar system.

## A/D and D/A Converter Stages

The front end accepts four full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into Linear Technology LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered to the Virtex-4 FPGA for signal processing or for routing to other module resources.

A TI DAC5686 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog output samples at up to 320 MHz to the 16-bit D/A converter. Analog output is through a front panel MMCX connector at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

## Core 428 Multiband DDCs

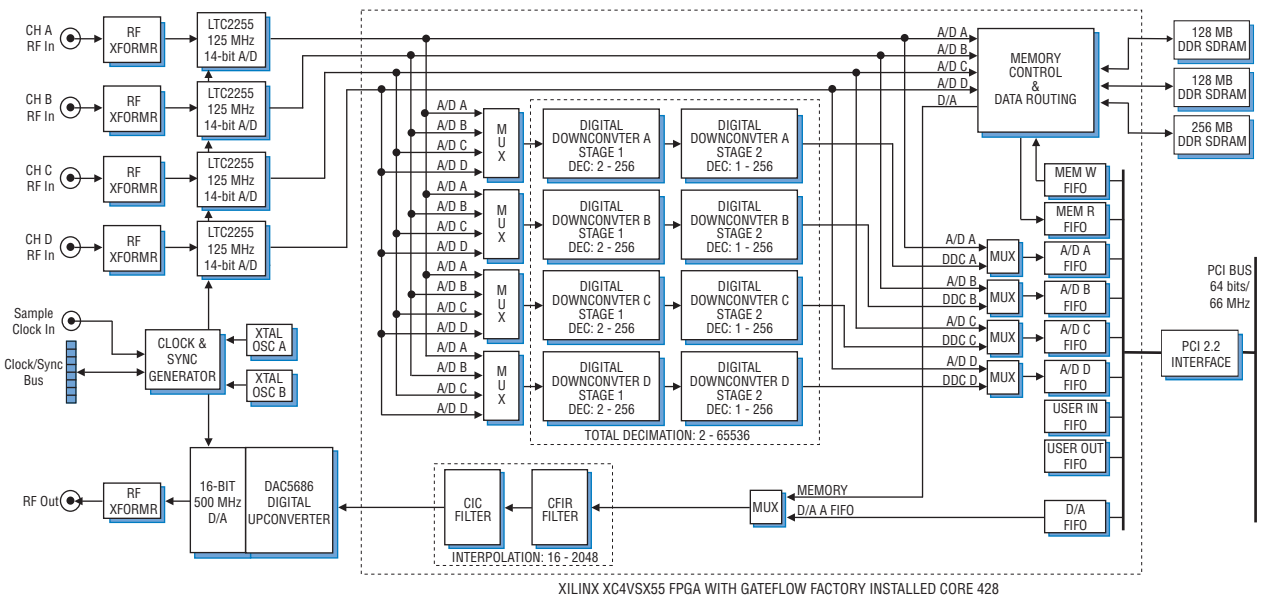
The Core 428 downconverter translates any frequency band within the input bandwidth range down to zero frequency. The DDCs consist of two cascaded decimating FIR filters. Each filter is capable of any decimation from 2 to 256. The decimations of the first stage filter and the second stage filter multiply to yield overall decimation factors up to 65,536. The second stage FIR may be bypassed for decimations of 256 or lower. The decimation of each DDC can be set independently. After each filter stage is a post filter gain stage. This gain is primarily used to compensate for bit growth in the filter at different decimations but may also be used to amplify small signals after out of band signals have been filtered out.

The NCO provides over 108 dB spurious-free dynamic range (SFDR). The FIR filter is capable of storing and utilizing two independent sets of 18-bit coefficients. These coefficients are user-programmable using RAM structures within the FPGA. NCO tuning frequency, decimation and filter coefficients can be changed dynamically.

Four identical Core 428 DDCs are factory installed in the 7142 FPGA. An input multiplexer allows any DDC to independently select any of the four A/D sources. The total decimation range from 2 to 65,536 provides output bandwidths from 50 MHz down to 1.52 kHz for an A/D sampling rate of 125 MHz and assuming an 80% filter.

## Core 428 Interpolation Filter

The Core 428 interpolation filter increases the sampling rate of real or complex baseband signals by a factor of 16 to 2048, programmable in steps of 4, and relieves the host processor from performing upsampling tasks. The interpolation filter can be used in series with the DUC's built-in interpolation, creating a maximum interpolation factor of 32,768.




XILINX XC4VSX55 FPGA WITH GATEFLOW FACTORY INSTALLED CORE 428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