Model 6821-422 Installed Core

GateFlow 215 MHz A/D and Digital Receiver - VME

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Features

- AD9430 12-bit 215 MHz A/D converter
- Dual GateFlow Core 422 296 MHz wideband DDCs, factory-installed
- Four sets of 18-bit user-programmable FIR filter coefficients
- Four FPDP or FPDP II front panel outputs
- FIFO buffering for real-time recording
- Xilinx Virtex-II Pro FPGAs
- ***Ruggedized and conduction-cooled versions available***

Ordering Information

Model	Description
6821	215 MHz, 12-bit A/D and Digital Receiver with Virtex-II Pro FPGAs - VME
Options:	
-050-422	Wideband 296 MHz DDC Core

General Information

Model 6821-422 GateFlow 215 MHz A/D and Digital Receiver is a high-frequency single channel A/D converter with built-in digital downconverters. It accepts one front panel analog input and delivers digital output samples over two or four FPDP connectors utilizing FPDP or FPDP II standards. LVDS I/O is also available.

The 6821 features an Analog Devices AD9430 12-bit A/D converter with a maximum sampling rate of 215 MHz. To convert this board into a complete software radio system, Pentek has added the GateFlow IP Core 422 High-Performance Wideband DDC similar in functionality to the Texas Instruments GC1012B, but with enhanced speed, performance and programmability.

In standard 6821 units, the Virtex-II Pro FPGAs contain factory-programmed code to implement control, initialization, mode selection and data formatting functions. Since most of the FPGAs remain available for custom algorithms, Pentek offers the 6821-422 as a factory installation of two complete channels of the GateFlow IP Core 422 (one channel per FPGA).

Architecture

The block diagram below shows the AD9430 A/D converter driving the Core 422 Wideband DDC, and also bypassing the DDC core for a direct connection to the output FIFOs.

The 6821-422 features up to four FPDP connectors for data output. Several data packing modes are selectable across the multiple FPDP ports.

Alternatively, LVDS I/O is available through either the VMEbus P2 connector or a second-slot front panel mezzanine.

Core 422 Digital Downconverter

The Core 422 DDC translates any frequency band within the input bandwidth range down to zero frequency, performs low pass filtering, and then combines and decimates the filter output for delivery as real or complex samples.

Pairs of consecutive even and odd input samples from the A/D are delivered to the core at half the sample clock frequency. An input gain stage allows scaling of the A/D data samples by a 16-bit gain term.

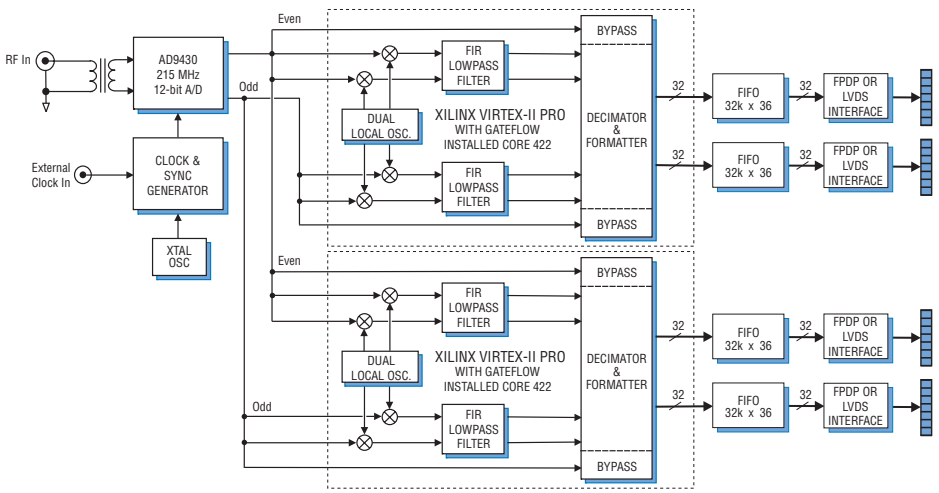
A dual complex NCO delivers pairs of even and odd complex local oscillator samples to four 18x18 multipliers which implement the complex mixer. The programmable NCO provides over 110 dB spurious-free dynamic range (SFDR).

The dual FIR lowpass filter can store and utilize up to four independent sets of 18-bit coefficients for each of six decimation settings: 2, 4, 8, 16, 32 and 64. Two default coefficient sets for 80% and 90% passband filters are also available:

Default Filter	Usable Bandwidth	Passband Ripple	Stopband Rejection
80%	0.8 Fs	< 0.08 dB	> 100 dB
90%	0.9 Fs	< 0.50 dB	> 75 dB

Fs = Complex Output Sample Rate

A DDC bypass path allows the A/D input data to be sent directly to the output formatting stage for delivery to the FPDP or LVDS outputs for data acquisition applications that require no downconversion.



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