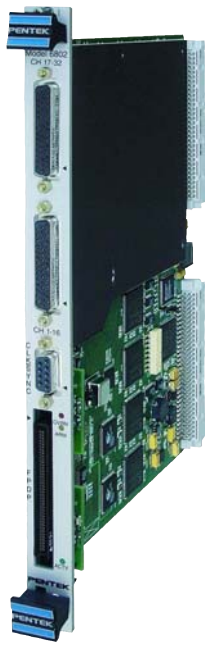
# Model 6802

# 32-Channel A/D with FPDP Output - VME



## Features

- Thirty-two sigma-delta A/D channels
- 24-bit accuracy
- Differential inputs
- Programmable gain amplifiers
- FPDP (Front Panel Data Port) output
- Sampling rates from 1 kHz to 216 kHz
- 100 kHz anti-aliasing filters
- Internal or external sample clock
- Front panel sync bus synchronizes all channels on multiple boards
- Single slot 6U VMEbus board

## Ordering Information

| Model | Description |
|---|---|
| 6802 | 32-Channel A/D with FPDP Output - VME |
| **Option:** | |
| -010 | Differential 10 V p-p full-scale input voltage |

## General Information

Model 6802 is a high-performance 32-channel A/D converter board capable of sampling rates up to 216 kHz. As a single-slot VMEbus board, the Model 6802 includes both signal conditioning and clock generation circuitry. Output samples are delivered to a FPDP connector.

## Signal Conditioning

The Model 6802 accepts 32 differential analog inputs with 16 channels on each of two front panel multipin connectors compatible with discrete wire termination.

Programmable-gain instrumentation amplifiers deliver each signal to a single-pole 100 kHz low pass anti-aliasing filter.

## A/D Conversion

Sixteen monolithic, dual-channel sigma-delta A/Ds provide 32 channels of A/D conversion. Each A/D features 24-bit resolution at sampling rates ranging from 1 kHz to 216 kHz. These A/Ds provide excellent channel-to-channel matching and linear phase response, ideal for sonar and acoustic applications.

## Sampling Control

The A/Ds utilize a high-speed system clock capable of 64x, 128x or 256x oversampling. This clock is sourced by an internal crystal oscillator or by an external clock supplied through a front panel DB9 connector. The internal oscillator can be replaced for custom sampling frequencies.

A programmable divider can be used to divide the internal or external system clock by a factor of 1, 2, 4, 8, 16, 32, 64 or 128.

## Synchronization

The front panel sync input signal allows synchronization of up to eight 6802 boards. In addition, the front panel connector provides trigger signal I/O for data collection in the on-board FIFO memory.

## FPDP Output

The number of active A/D channels can be selected from 1 to 32 in steps of 1. Data samples from all selected channels are then interleaved and stored in a 32-bit wide FIFO memory as either one 24-bit sample or two packed 16-bit samples.

The FIFO delivers samples from all selected channels to the FPDP output using 30 MHz PECL or 20 MHz TTL strobes.

## Specifications

**Input:** differential, 2.4 V p-p full scale, DC coupled, each input 10 kohm to ground
**Gain:** 1, 10 or 100
**Anti-aliasing filter:** lowpass, $f_c$=100 kHz
**A/D converters:** 24-bits, AKM AK5394, SNR >90 dB, THD <–100 dB FS
**Sample Rate**: 1kHz to 216 kHz
**System Clock:** internal 12.800 MHz crystal oscillator, or external TTL clock via front panel connector (64 kHz to 13.824 MHz)
**System Clock divider:** divides internal or ext. clock by 1, 2, 4, 8, 16, 32, 64 or 128
**Output:** FPDP, 32-bit, 30 MHz PECL strobe or 20 MHz TTL strobe
**VME Interface**
**Type:** slave A16 D16
**Control:** gain, channel selection, filters, operating modes, resets, data packing
**Size:** 6U board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 0.8 in. wide