New!

Model 6526

16-Channel 2-Input RACEway Digital Receiver Board

Preliminary Information

Features

- Two 16-bit TTL or ECL front panel A/D inputs
- Sampling rates to 62.5 MHz
- Fully programmable receiver tuning and decimation
- 160 MB/sec RACEway outputs
- Each RACEway packet contains data from one receiver channel only
- Multiple board channel synchronization for beamforming applications
- On-board input channel switch generator
- FIFO Buffering
- On-board time code generator for time stamping
- Compatible with Pentek 4290 and 4291 Quad 'C6x DSP's and 4285 Octal 'C40 DSP with RACEway I/F
- Compatible with Pentek Series 64xx A/D Converters

General Information

Model 6526 is a 16-channel 2-input narrowband digital receiver for VMEbus. It features a RACEway interface for output data and several on-board control sections for supporting input switching, multiple board synchronization and time code stamping of data.

Model 6526 is a single-slot 6U VME board with front panel connections for input clock, data and synchronization signals. It includes a 32-bit VMEbus slave interface for control and status.

The RACEway interface allows packets of data from each receiver channel to be directed to different RACEway-equipped VME boards including boards with memory and DSP functions.

Digital Receiver

The Model 6526 utilizes four Graychip GC4014 quad narrowband digital receiver chips to provide a total of 16 receiver channels. Two front panel parallel data inputs are accepted on a multipin ribbon cable connector.

The parallel inputs operate at either TTL or differential ECL logic levels and support up to 16 bits of data and one clock at sampling rates up to 62.5 MHz for ECL and up to 50 MHz for TTL. Both inputs must operate at the same clock speed. The front panel inputs are directly compatible with Pentek's Series 64xx A/D converters.

The two parallel input signals are connected to two inputs of each GC4014. Within the GC4014, input crossbar switches allow any receiver channel to independently select either of the two input signals.

The GC4014s are controlled by commands from the VMEbus and by a local receiver command controller for setting all operational parameters of the receiver channels.

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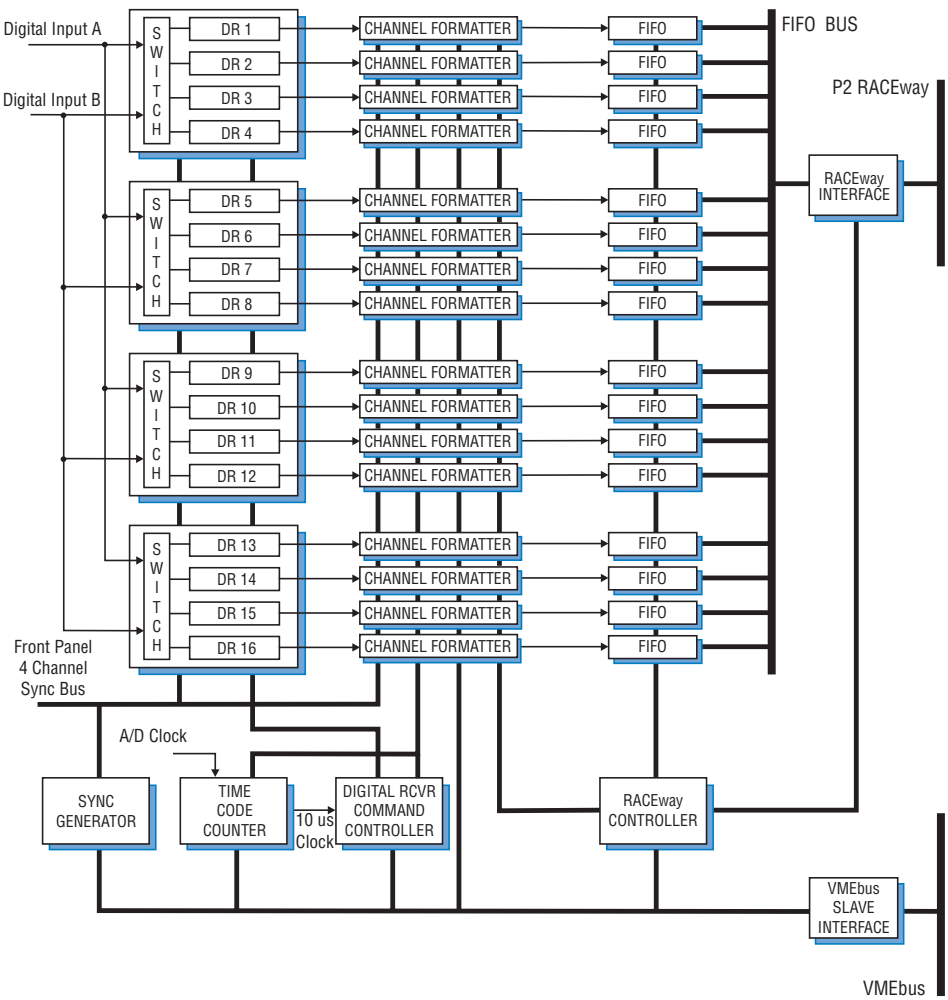
Block Diagram, Model 6526



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Model 6526

16-Channel 2-Input RACEway Digital Receiver Board

A front panel sync bus consisting of a parallel multiconductor ribbon cable, bridges across all Model 6526s in a system and utilizes the same style connectors as the digital inputs. The bus is used to distribute 4 synchronization signals to all connected boards for synchronizing each of the same-numbered channel receiver sections on each board. An on-board sync generator controlled by VMEbus commands can generate any number of sync signals for output to the sync bus.

Time Code Generator

A 32-bit time code counter acts as a master time code reference for the board. It is used for time-stamping data packets from the receivers and for determining when input switching commands are performed. It advances its code using a nominal 10 µsec clock derived by dividing (prescaling) the input clock from the parallel digital input.

Command Controller

A receiver command controller utilizes a list of input channel switching times for each of the 16 channels. This list is written through the VMEbus interface into a table and then examined once every 10 µsec to determine if any receiver channel should change its input switch setting for the current 32-bit time code.

Channel Formatter

Sixteen identical channel formatter sections accept serial output data from the GC4014, convert the data to 32-bit parallel words and then form data packets (blocks) containing channel identification, the block number, the time code value, and a programmable number of complex receiver data samples. The channel identification and block counter values are programmable over the VMEbus interface.

Optionally, the channel formatter also inserts a special sync code pattern in the data sequence. This pattern replaces a programmable number of receiver samples, after receipt of the sync bus signal for that channel.

The channel formatter also stores the RACEway routing code and RACEway address for each channel in VME-programmable registers. This allows each channel's data packet to be directed to any RACEway board and then steered to any resource within the board.

Data packets from the channel formatter are delivered to 4k x 32 synchronous FIFO's, one for each of the 16 channels. Once a data packet is delivered to a FIFO, a signal is sent to the RACEway controller which then retrieves the RACEway routing code and address from the channel formatter and starts a RACEway bus transfer using the packet stored in the FIFO.

VME Interface

The VMEbus slave interface allows read/write control of every programmable function register and memory. These resources are memory mapped into an A24/A32 VME address space. A second address space, identical to the first, provides write-only access to the same functions.

The base addresses of each of these two spaces are programmable over A16 address space. This allows multiple boards to share the same write-only space for broadcast commands sent to several boards using a single VMEbus cycle. Individual board commands can always be sent through the read/write space.

Compatibility

Model 6526 is directly compatible with the Pentek Models 4290 and 4291 Quad TMS320C6x DSP Processors and 4285 Octal TMS320C40 DSP Processor with their optional RACEway interfaces. The 6526 supports local RACEway packet steering to any of the four processors, as determined by the RACEway address.

Ordering Information

Model	Description
6526	16-Channel 2-Input Digital Receiver VME board with RACEway interface
Options	
-002	Differential ECL inputs
-019	Single-ended TTL inputs