Model 6251

Virtex-II Pro FPGA Configurable Logic and I/O - VIM-2

ReadyFlow Board Support Package

GateFlow

Features

- Supports high-performance custom signal processing
- One or two FPDP or LVDS I/O front panel interfaces
- Xilinx Virtex-II Pro FPGAs
- FPGA configuration package includes VHDL source code and design examples
- FPGA configuration code can be downloaded from processor nodes or stored in non-volatile EEPROM
- On-board auxiliary SDRAM and FLASH memory
- Factory-installed cores available

General Information

The Model 6251 is a Configurable Logic FPGA VIM-2 (Velocity Interface Mezzanine) module with optional FPDP (Front Panel Data Port) or LVDS I/O. It features one or two front panel interfaces, and two Xilinx Virtex-II Pro FPGAs.

As a VIM-2 module, Model 6251 connects to one of the two VIM-2 sites on a VIM baseboard, leaving the other site available for a second VIM-2 module of any type.

FPGA Devices

The Model 6251 is equipped with two of several FPGA devices in the Xilinx Virtex-II Pro family including Models XC2VP20 and XC2VP50 (selectable by option number). Contact factory for alternate sizes.

Each FPGA interfaces directly to all three sections of the associated VIM interface: the serial ports, 32-bit BI-FIFO parallel port and control/status port. The VIM BI-FIFO buffers on the processor board allow the processors to move blocks of data efficiently to and from each FPGA.

The two FPGAs are interconnected with 84 programmable user I/O lines to support data, clocking and control passing between the two devices.

Memory

Each FPGA is equipped with a 16M x 32 (64 MB) SDRAM connected with separate address and data buses so it can be used independently. These SDRAMs are useful for storing data without consuming internal FPGA logic cells. In addition, 16 MB of FLASH memory is attached to each FPGA, for a total of 32 MB.

Front Panel I/O Interfaces

The 6251 offers several configurations of front panel FPGA I/O. First, an optional multipin front panel connector provides LVDS I/O in the first slot (option -007), or in an adjacent slot (option -122). These options can be combined to obtain LVDS I/O from both of the on-board FPGAs.

An additional I/O solution is the optional FPDP interface in the first slot (option -008), or an adjacent slot (option -014). These options can be combined to obtain FPDP I/O from both on-board FPGAs. Alternatively, option -008 can be combined with option -122 to achieve both FPDP and LVDS I/O simultaneously.

These numerous 6251 front panel possibilities are achieved by the use of unique Pentek "personality modules". This flexible design makes it possible for a user to create custom I/O modules.

FPGA Programming

Pentek's optional GateFlow Design Kit allows the FPGAs to be configured by the user for implementation of custom preprocessing functions such as FFTs, FIR filters, compression and decompression algorithms, software radio blocks, decryption, decoders and encoders, and convolution.

The GateFlow FPGA Design Kit is used in conjunction with the Xilinx Foundation development tool suite, and includes VHDL source files for the VIM interface and control registers for clock functions. Templates for implementing custom signal processing blocks are also included. FPGA code may be loaded from the processor or permanently stored in non-volatile memory.

Ordering Information

Model	Description
6251	Configurable Logic & I/O with Virtex-II Pro FPGA - VIM-2
Options:	
-007	First-slot LVDS I/O
-008	First-slot FPDP I/O
-014	Second-slot FPDP I/O
-020	XC2VP20 FPGAs
-050	XC2VP50 FPGAs
-122	Second-slot LVDS I/O
-340	64 MB SDRAM and 16 MB FLASH per FPGA