Model 6236

14-bit A/D Converter with FPGA and Optional DDCs - VIM-2

ReadyFlow Board Support Package

GateFlow

Features

- Two low distortion 105 MHz 14-bit A/D converters
- Internal or external A/D sample clock to 105 MHz
- Advanced Virtex-II FPGA for signal preprocessing
- Front panel sync bus
- ASIC and FPGA wideband downconverter options

General Information

Model 6236 is a dual 14-bit A/D VIM-2 module. It attaches directly to VIM-compatible baseboards and includes a Virtex-II FPGA (Field Programmable Gate Array) as well as optionally available wideband digital receivers.

Front End

The Model 6236 accepts two analog RF inputs at +4 dBm full scale into 50 ohms on front panel SMA connectors.

Each of the two inputs is transformer coupled and digitized by an Analog Devices AD6645-105 14-bit A/D converter. The AD6645 is capable of operating at sample rates from 30 MHz to 105 MHz.

The A/D converter clock can be driven from an internal crystal oscillator or from an external sample clock supplied through a front panel SMA connector or front panel sync bus.

FPGA

The A/D outputs are delivered to a Xilinx Virtex-II FPGA (Model XC2V1000 standard; XC2V3000 optional) which is factory configured to perform various modes of data packing, formatting and channel selection. The A/D outputs are connected directly to the FPGA so that wideband A/D data can be delivered directly to the DSP board.

Optionally available design kits allow the FPGA to be configured by the user for implementation of custom preprocessing functions such as convolution, framing, pattern recognition and decompression.

Optional Digital Downconverters

The 6236 offers two different wideband digital downconverter options, each featuring a decimation range from 2 to 64.

Option -212 adds two bypassable Graychip GC1012B downconverter ASICs with 40 MHz maximum bandwidth for a 100 MHz sample clock, 75 dB stopband attenuation, 12-bit input and 16-bit output.

Option -421 adds a dual-channel GateFlow Downconverter Installed Core within the FPGA with 42 MHz maximum bandwidth for a 105 MHz sample clock, 100 dB stopband attenuation, 14-bit input, 24-bit output and programmable filter coefficients.

Synchronization

The front panel clock and sync bus allow one 6236 to act as a master driving the sample clock out to a front panel cable bus using LVDS differential signaling. Multiple slaves can then be clocked synchronously with the master.

Front Panel I/O

An optional front panel connector provides digital input and output for the FPGA. These lines are available for triggering, synchronizing, or framing signals. They are also useful during FPGA algorithm development for timing and signal probing.

VIM Processor Interface

The FPGA outputs are connected directly through the VIM mezzanine interface to the 32-bit synchronous BI-FIFO on the VIM processor board where it is buffered for efficient block transfers into the DSP.

Ordering Information

Model	Description
6236	14-bit A/D with FPGA and Optional Downconverters - VIM-2
Options:	
-102	Front panel FPGA I/O (additional slot)
-212	Two ASIC Graychip GC1012B Wideband Digital Downconverters
-421	GateFlow Wideband 2-Ch Digital DDC Core in FPGA
-300	Xilinx XC2V3000 FPGA replaces XC2V1000