Model 4954-422 GateFlow IP Core

GateFlow Wideband Ultra High-Speed DDC IP Core

For more information go to:
pentek.com/fpga

Features

- Ultra high-performance wideband digital down-converter (DDC)
- Supports Virtex-II™ and Virtex-II Pro™ FPGAs
- Fits in Virtex-II XC2V3000 or larger
- Similar to GC1012B with enhanced features
- Dual, demultiplexed inputs for 16-bit real or 16-bit complex (I and Q) data
- Maximum input data rate of 296 MHz for a 148 MHz clock
- Fully programmable dual NCO with 32-bit frequency and phase offset control
- SFDR >110 dB
- 2, 4, 8, 16, 32, and 64 decimation for complex output
- 1, 2, 4, 8, 16, and 32 decimation for real output
- Dual decimating FIR filter features up to 1792 taps
- Four sets of programmable 18-bit FIR filter coefficients
- Default FIR filter coefficients for 80% and 90% filters
- Output formatter delivers real, complex, offset, inverted data in 16 or 24 bits

Ordering Information

Model	Description
4954-422	Wideband Ultra High-Speed DDC IP Core

General Information

The Pentek GateFlow Model 4954 Library IP Core 422 is a high-speed wideband digital down-converter (DDC) designed specifically for Xilinx Virtex-II and Virtex-II Pro FPGAs.

The core employs a dual DDC architecture accepting two demultiplexed inputs suitable for new high-speed devices such as the AD9430 215 MHz 12-bit A/D.

The core offers similar functionality to the Texas Instruments GC1012B, but with enhanced speed, performance and programmability. The core consists of three major DSP sections: the mixer, the local oscillator and the FIR filter.

Dual Input Stage and Dual NCO

Two 32-bit data input ports accept odd and even complex samples in parallel at up to 148 MHz. Inputs can be scaled by a 16-bit gain multiplier, and overflow logic detects overflows.

The dual NCO (numerically controlled oscillator) local oscillator generates two cosine and sine sequences which are applied to the dual complex mixer to translate the input signal to zero frequency. This NCO provides over 110 dB spurious-free dynamic range (SFDR). Additional logic provides more flexible frequency and phase control as well as independent accumulator reset.

Dual Mixer and FIR Filter

The dual mixer utilizes eight 18 x 18-bit multipliers to handle the two complex inputs from the NCO and the two complex data input samples. For real input data, the two Q input paths are simply set to zero.

A mixer bypass path allows input data to be sent directly to the FIR filter with no frequency translation.

The dual FIR low-pass filter operates on the two mixer outputs to remove energy from adjacent channels. It uses a highly-efficient proprietary polyphase decimating filter architecture with decimation factors of 2, 4, 8, 16, 32, and 64.

Output Stage

The output formatter allows the user to invert the output spectrum; to offset the spectrum by one-half the output rate; to convert the complex output stream to a real stream at twice the rate; and to round the output to 16 or 24 bits.

Speed Performance

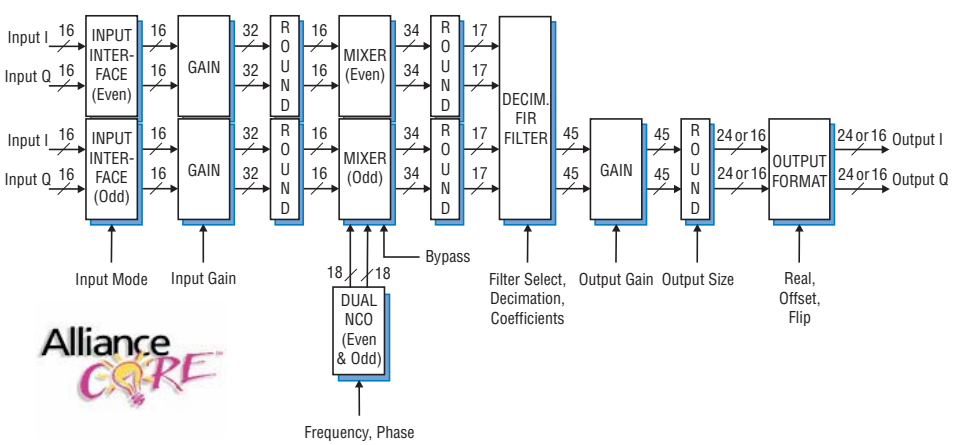
Input and output sampling rates are proportional to the clock frequency. The maximum clock frequency for each device is determined by its speed grade.

Xilinx Speed Grade	Max Clock Rate	Max Input Sample Rate
-7	148 MHz	296 MHz
-6	140 MHz	280 MHz
-5	126 MHz	252 MHz
-4	110 MHz	220 MHz

FPGA Resource Utilization

The Core 422 will fit into the Xilinx Virtex-II XC2V3000 or larger devices. The chart below shows the utilization of FPGA resources:

Resources	Core 422
Slice LUTs	9,758
Slice Flip-Flops	12,921
Block RAM	74
Block Multipliers	72
Global Clocks	2



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