Model 4474

14-bit 10 MHz A/D Converter VXI Module

Features

- 14-bit A/D converter with integral sample-and-hold
- 10 MHz maximum conversion rate
- TMS320C40 DSP communications port output
- 512 ksample, high-speed data buffer memory
- Internal or external sampling clock
- Includes platform-independent VI driver for National Instruments LabVIEW
- VXI*plug&play* compliant

Ordering Information

Model	Description
4474	14-bit 10 MHz A/D VXI module

General Information

This high-performance A/D converter VXI module with extremely deep on-board memory serves as ideal front end for wide-band data acquisition and signal analysis systems. The dual output capability, using either the 32-bit VXIbus or the 8-bit TMS320C40 front panel comm port, supports many different signal processing requirements and architectures.

A/D Conversion

The heart of the unit is an integrated sample-and-hold amplifier and A/D converter delivering 14-bit resolution at a 10 MHz sampling rate. An input overload condition is detected and latched so that the processor may be warned of a data block of compromised integrity.

Flexible Buffer Memory and Outputs

Two 256k x 16-bit data buffers have been arranged in a "swinging buffer" configuration. One buffer is connected to accept data from the A/D converter at a 10 MHz maximum data rate. The second buffer is available to provide sequential samples to the VXIbus, or the front panel 'C40 comm port and behaves like a FIFO (first-in-first-out) memory.

When both buffers have completed their operation cycles, the buffers may be configured to automatically swap for the next cycle. This arrangement supports two completely independent data rates for the A/D converter and the output interface.

Sample Clock Oscillator

A crystal-controlled DIP oscillator is provided for use as the sample rate clock source. The oscillator is socketed and user-replaceable for operation at virtually any frequency up to 10 MHz. Alternately, a front panel BNC connector accepts an external TTL clock.

Specifications

Input: ±2.0 V full scale, front panel BNC, 50 ohms input impedance

A/D converter: 14-bits up to 10 MHz with integral sample-and-hold (Edge Technology ET2471)

Trigger/Gate control TTL-compatible input, or VXIbus control bit; positive or negative edge starts conversion; logic '0' or '1' enables conversion; generates VXIbus interrupt N samples after trigger, where N = 1 to 256

Data memory buffer: two each, 256k x 16 (256k samples) max. size; binary-step control from 1k to 256k, software configurable; swinging buffer scheme, provides up to 512k contiguous sample storage; output buffer appears as a FIFO mapped to a single memory location

VXI interface: A16/A24/D16/D32 device; memory-mapped registers for status and control; all data transfers in and out of the module are buffered in the 2 MB local SRAM which is mapped to the VXIbus

'C40 comm port interface: two 8-bit bytes per sample, high byte first; 20 Mbytes/sec output rate

Power: 5.0 A at +5 V; 0.5 A at +12 V; 0.5 A at –12 V; 0.5 A at –5 V from the VXIbus

Size: standard C-size VXI module

Block Diagram, Model 4474