Model 4254: Single
Model 4257: Dual

Single or Dual TMS320C40 Coprocessor MIX Modules

Features

- Floating-point DSPs, with up to 100 MFLOPS peak processing power
- 1 MB local SRAM per processor and 1, 2 or 3 MB global SRAM
- 32 kB EPROM per processor

SwiftNet

Ordering Information

Model	Description
4254	Single TMS320C40 Coprocessor MIX module, 40 MHz clock
4257	Dual TMS320C40 Coprocessor MIX module, 40 MHz clock
Options	
-002	2 MB Global SRAM
-003	3 MB Global SRAM
-015	50 MHz clock

General Information

For very demanding, computation intensive applications, TMS320C40 Coprocessor MIX Modules provide additional processing power. Model 4254 is a single and Model 4257 is a dual 'C40 Coprocessor MIX expansion modules.

When stacked on a Model 4284 'C40 Processor VMEbus MIX Baseboard, Model 4257 provides an additional 100 MFLOPS of processing power, while Model 4254 provides an additional 50 MFLOPS. In these cases, the baseboard processor moves programs and data between the coprocessor module and other MIX modules, and the VMEbus backplane.

Using the Models 4200–4202 MIX Baseboards unleashes the MIX bus master capabilities of these models allowing them to move data between other MIX modules. The Model 4200 MIX Baseboard extends their power to full bus master operation for both VMEbus and VSBbus.

High Speed Communications

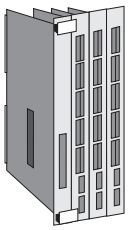
The 'C40 is provided with six ports for high speed communication with other devices or 'C40 processors. Each port is capable of 20 MB/sec asynchronous bidirectional transfer for maximum communication flexibility. Five of these ports from each processor are brought out to front panel connectors, while the sixth one is connected between processors. The sixth port is unused in the 4254. In addition, a J-TAG Texas Instruments XDS emulator connector is available on the front panel.

Parallel Arrays

Using three of these modules, up to six 'C40s can be configured per subsystem for parallel multiprocessor applications:

- arrays for 3-D image processing
- bidirectional rings for neural networks
- pipelined linear arrays
- tree structures for complex searches
- hexagonal grids for numerical analysis
- 4-D hypercube structures

350 MFLOPS DSP System

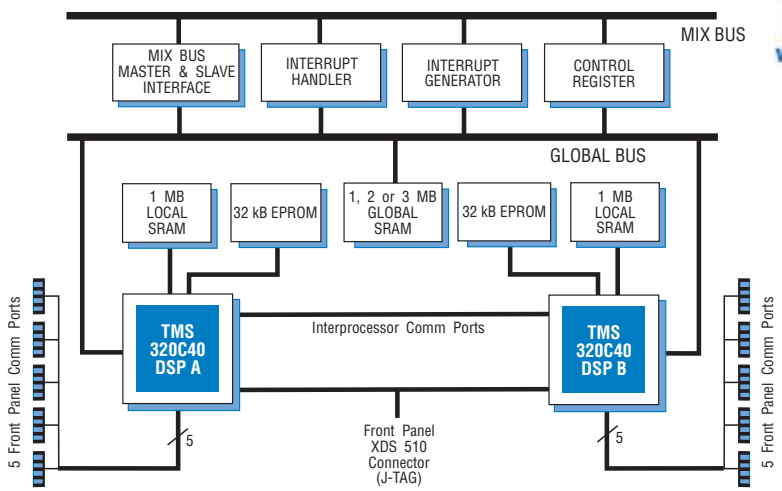


Three Model 4257s attached to a Model 4284 make a 350 MFLOPS DSP engine in four VMEbus slots. The 4284 Baseboard serves as the system executive for program control and data flow.

Specifications

Processors: One or two TMS320C40, 40 or 50 MHz clock
Local SRAM: 256k x 32 (1 MB) per processor, zero wait state for data and programs; access through local bus
EPROM: 32 kB per processor
Global SRAM: 256k x 32 (1 MB), one wait state accessible from either 'C40's global bus and the MIX interface; optionally expandable to 2 or 3 MB
Comm ports: five front panel bidirectional ports per processor, 20 MB/sec
MIX interface: master and slave
Power: Model 4254 1.1 A at +5 V from the MIX bus; Model 4257 1.9 A at +5 V from the MIX bus

Block Diagram, Model 4257



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