Model 4241

Parallel Digital I/O MIX Module

Features

- Parallel 32-bit data with 4-bit addresses
- Targets successive data blocks to specific processor boards for parallel FFT or multiband digital FIR filter calculation
- Can cascade two or three modules for decimating filtering or data reduction
- 10 Msample/s input and output data rates
- 1–16 ksample FIFO buffers the 32-bit input data

Ordering Information

Model	Description
4241	Parallel I/O MIX module
Option:	
-001	8 ksample FIFO
-002	16 ksample FIFO

General Information

Using a full 32-bit parallel data word for both input and output, Model 4241 Digital I/O MIX Module serves as a slave device to transfer digital data from its front panel connectors to one or more subsystem processors via the MIX bus. Although often combined with other MIX modules, up to three digital I/O modules may be used in a subsystem for applications such as decimating filters or data reduction, where the output of one I/O feeds the input of another. The module nests on a MIX baseboard, so that together they occupy only a single card cage slot.

Simpler Multiprocessor Systems

The simple data transfer scheme employed by the module facilitates the implementation of multiprocessor systems. For example, in high speed FFT calculation, successive blocks of data can be passed to several Model 4284s without any impact on host bus bandwidth.

Selective Parallel 32-bit Data Inputs

The front panel input connection to the module accepts 32-bit parallel data and its associated 4-bit address. A dip switch allows the module to accept only data accompanied by a preset address or all data. Data may thus be targeted to specific processor boards in a multiprocessor system.

More than one digital I/O module input can be written to in parallel from any digital output device that provides a data-valid strobe. Such output devices include the Pentek Model 4261 A/D Converter and other digital I/O modules. A FIFO buffers data between the input data register and the MIX interface.

Targeted Digital Output

Digital output operation is achieved by writing to a 32-bit output data latch, memory-mapped into the baseboard processor's memory space via the MIX interface. A 4-bit address latch targets the receiving device. Straightforward handshake protocol notifies the initiating processor when data has been accepted.

Specifications

Input and output data: 32 bits, TTL/+5 V CMOS, single-ended
Handshake: 2-wire handshake, NDAC and DAV
Input FIFO: 1k x 32 expandable to 16k x 32 bits with full, half-full and empty flags
Input and output data rate: 10 Msamples/sec
Input address comparator: 4 bits set with on-board DIP switches; compare can be disabled
Output: 32-bit data and 4-bit address latches
MIX interface: interrupt mask register, status/control register, input FIFO, output data latch and output address latch are all memory-mapped on MIX bus
Power: 0.7 A at +5 V, from the MIX bus

Block Diagram, Model 4241