Model 7656

Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PCI

ReadyFlow Board Support Package

GateFlow

Features

- Complete software radio interface solution
- Two 400 MHz, 14-bit A/Ds
- One digital upconverter
- Two 800 MHz, 16-bit D/As
- Up to 1 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Dual timing buses for independent A/D and D/A clock rates
- LVPECL clock/sync bus for multiboard synchronization
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Model 7656 is a half-length PCI board that includes two 400 MHz A/Ds, 800 MHz D/As and Virtex-5 FPGAs. It consists of one Model 7156 mounted on a PCI carrier board. The Model 7656 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into TI ADS5474 14-bit 400 MHz A/Ds. Designed with a 750 MHz input bandwidth, the A/Ds are excellent for undersampling applications.

The digital outputs are delivered into the Virtex-5 processing FPGA for signal processing, data capture or routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 300 MHz. It delivers real or quadrature (I+Q) outputs at up to 500 MHz to the 16-bit D/A converter. Analog output is through a pair of front panel SMC connectors at +4 dBm into 50 ohms. If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

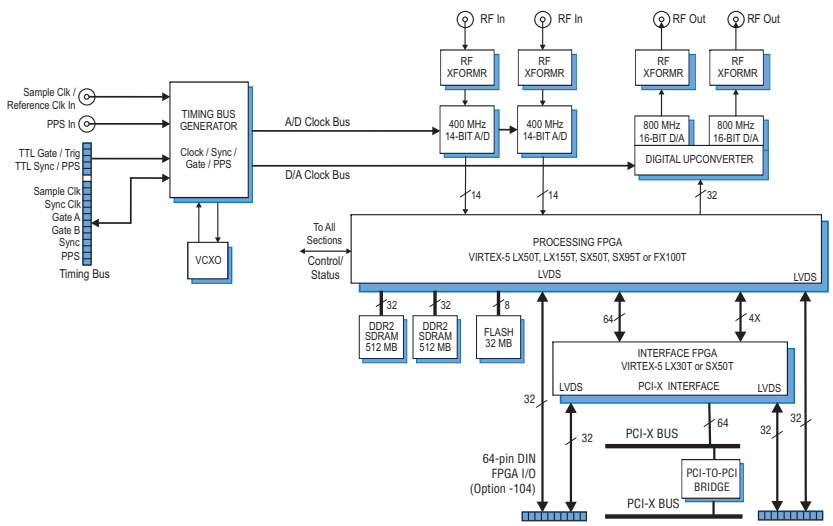
Virtex-5 FPGAs

The Model 7656 architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the data converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T, and FX100T.

The SXT parts feature between 288 and 640 DSP48E slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay, and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the board can be optionally configured with an LX155T in the processing FPGA position for 156,648 logic cells.

A second Virtex-5 FPGA provides the board's PCI-X interface. Implementing the interface in this second FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT family or an SXT family part, providing not only interface ➤



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➤ functionality, but processing resources up to an additional 640 DSP48E slices.

Option -104 adds a 64-pin DIN connector with 16 pairs of LVDS connections to each FPGA for custom I/O.

Clocking and Synchronization

Two internal timing buses can provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An internal clock generator receives an external sample clock from the front panel SMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SMC connector can be used to provide a 10 MHz system reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to three slave 7656's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Up to two independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and D/A waveform playback mode. All memory banks are supported with DMA engines for easily moving data through the PCI interface.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI-X Interface

The Model 7656 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33, 66 and 100 MHz are supported.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SMC connectors
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 250 kHz to 750 MHz

A/D Converters
- **Type:** TI ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

D/A Converters
- **Type:** TI DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 300 MHz
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with intepolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female SMC connectors
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 250 kHz to 750 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer:
- **Clocks Source:** Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus
- **Synchronization:** Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock
- **Type:** Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms, accepts 20 to 400 MHz sample clock or 10 MHz system reference
- **Timing Bus:** 26-pin connector LVPECL bus includes clock/sync/gate/PPS input/output; TTL signals for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays
- **Processing FPGA:** One Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VFX100T, or XC5VLX155T
- **Interface FPGA:** One Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T or XC5VFX70T

Custom I/O
- **Option -104:** Installs the P14 connector with 16 LVDS pairs to the processing FPGA and 16 pairs to the interface FPGA mapped as two 16-bit read/write registers

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7656	Dual 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PCI
Options:	
-104	FPGA I/O through a 64-pin DIN connector

Contact Pentek for additional available options.

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