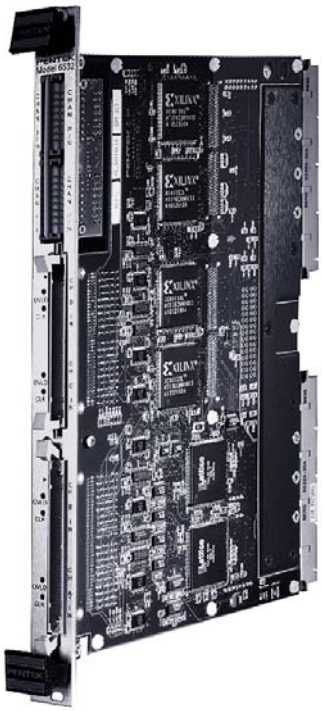
Model 6532

32-Chan. 4-Input Narrowband Digital Receiver VME Board



General Information

Model 6532 is a general purpose multi-channel digital receiver VME board which accepts digitized data from four parallel inputs at sampling rates up to 62.5 MHz. Configured with 32 channels of narrowband receivers, it performs frequency downconversion, lowpass filtering and decimation of the sampled output. Each of the 32 receivers can independently select any one of four input sources.

The receiver output signals are first processed in a FPGA (field-programmable gate array) which performs serial-to-parallel conversion as well as some simple, high-speed preprocessing tasks including summation of multiple channels for beamforming applications.

The FPGA outputs are then sent into FIFO memory buffers up to 64k samples deep. The FIFO outputs can be read by an on-board TMS320C40 DSP processor which is capable of performing demodulation, decryption, and other signal analysis tasks; alternately they can be output to four hardware comm ports.

Receiver Chips

Model 6532 utilizes the highly-integrated Graychip type GC4014 quad digital receiver chip containing four receiver sections, each with a tunable local oscillator, mixer and programmable low pass output filter.

Each GC4014 accepts all four front panel parallel inputs and an internal cross-bar switch allows each receiver channel to independently source data from any of these four inputs.

The parallel inputs operate at differential ECL logic levels and support 14 bits (four inputs) or 16 bits (three inputs) of data at sampling rates up to 62.5 MHz for ECL or 40 MHz for FPDP.

The output formatting section of the GC4014 includes both real and complex output modes as well as a summation mode which sums the four output channels for beamforming applications.

The multiplexer control, local oscillator frequency and the output filter cutoff frequency in each receiver are independently programmable by the C40 DSP or over the VMEbus interface, providing extremely flexible and agile operation.

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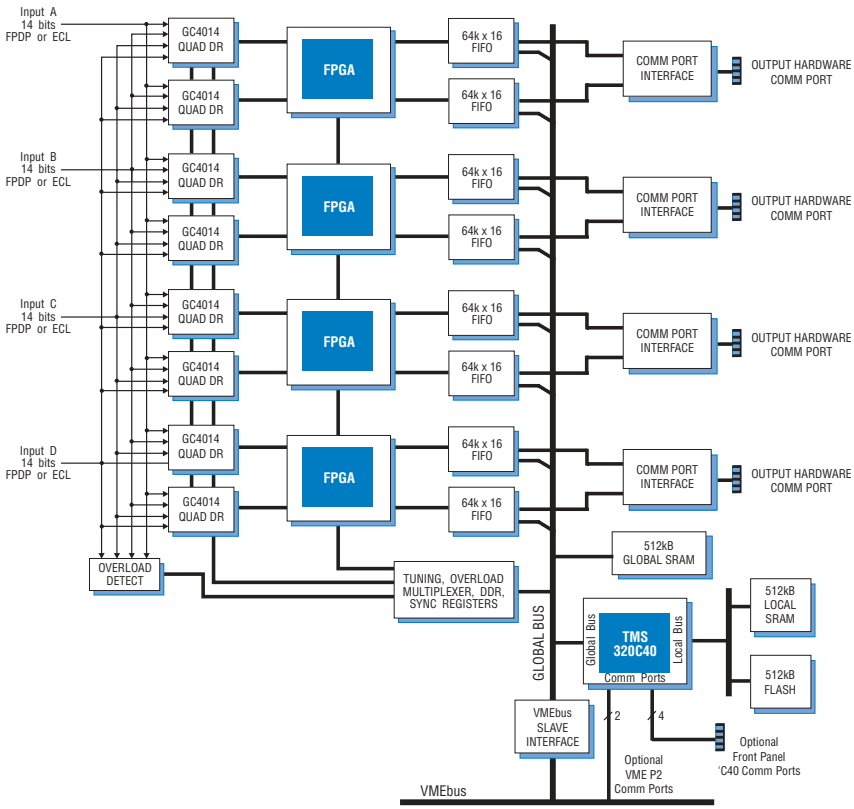
Block Diagram, Model 6532



Features

- Four 14-bit or three 16-bit A/D inputs via ECL or FPDP
- Sampling rates to 62.5 MHz
- On-board C40 DSP
- FPGA preprocessor supports summation of up to eight channels for beam-forming applications
- Four front panel C40 comm ports
- Two C40 comm ports for VMEbus P2 (optional)
- Dynamic range to 100 dB
- ~0.015 Hz tuning resolution
- Up to 64k FIFO buffering
- Compatible with Pentek's Series 64xx A/D Converters

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Flexible Input Connections

All input data is accepted on front panel parallel digital connectors with differential ECL level compliance or FPDP connectors.

An input overload detector on each input can be used to generate interrupts to the C40 to indicate near full scale digital samples.

TMS320C40 DSP Processor

The C40 DSP can be used to perform signal processing tasks, and also simply as a data distribution engine for sending data out through the front panel comm ports (Opt. -036). It features two 512kB zero-wait state SRAMs, one on the local bus and one on the global bus.

Front Panel Comm Ports - Hardware

Four comm ports suitable for connection to external C40 processors are provided for sending data from the 6532's FIFOs directly out through the front panel. This is the standard configuration, and does not provide any direct connection to the board's C40 processor.

Front Panel Comm Ports - C40

With option -036, the four front panel C40 comm ports are directly connected to the 6532's C40 processor. This allows such operations as preformatting data before transmission, etc.

Alternatively, option -035 provides two C40 comm ports brought out to rows A and C of the VMEbus P2 connector. This option can be used to add direct C40 comm port connection while maintaining the front panel hardware comm port connection.

Combining Multiple Boards

Two Model 6532's can be joined such that the GC4014's on both boards are synchronized.

The synchronization, clocking and data signal lines are routed over a flexible ribbon cable through front panel connectors.

Specifications

Narrowband Receivers (32)

Receiver type: (8) Graychip GC4014's

Digital input format: four independent inputs; each input with 14- or 16-bit words, 2's complement; one sample rate clock line

Input levels: Must specify option
FPDP (option -008)
ECL differential (option -012)

Sampling rate: up to 40 MHz max (FPDP) or 62.5 MHz max (ECL)

Data input connectors: dual 80-pin flat ribbon cable 0.025" pitch (3M)

Input multiplexers: each receiver channel can independently select one of four front panel inputs under program control

Local oscillator: direct digital synthesizer; frequency = $F*f_s/2^{32}$, where F is a 32-bit binary integer and f_s is the input sample rate

Tuning range: DC to $f_s/2$ (31.25 MHz for f_s = 62.5 MHz)

Tuning resolution: $f_s/2^{32}$ (~0.015 Hz for f_s = 62.5 MHz)

Low pass filter: decimating FIR programmed by 14-bit integer D, from 8 to 16,384; nominal output Nyquist bandwidth $f_N = f_s/4D$; output sampling rate is $f_s/4D$ for complex outputs and $f_s/2D$ for real outputs

FIR filter: 63 taps symmetrical, 32 taps non-symmetrical, 16-bit coefficient

Fixed FIR: ±0.05 dB passband ripple to $0.8f_N$ (default coefficients)

Real mode: 16-bit real output samples at sampling rate $f_s/2D$

Complex mode: 16-bit complex (interleaved I and Q) output samples at sampling rate $f_s/4D$ per complex pair

Data FIFOs (8): 16k x 16; optionally 32k x 16 (option -023) or 64k x 16 (option -024); VME and C40 interrupts for full, half-full and empty

Data Routing: the FPGA distributes data from each GC4014 receiver output into its associated FIFO; alternately, the data from each GC4014 pair can be summed to a single associated FIFO (Summing Mode)

Comm Port Outputs: optionally four front panel (option -036) plus two on VME P2 (option -035) from internal C40

Control registers: memory-mapped over the VMEbus and local bus of C40; receiver chip control registers (includes local oscillator, data packing, clock multiplier, filter decimation, real/complex mode, etc.), crossbar multiplexer, and channel synchronization control

Size: standard 6U VMEbus board, single slot; board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 0.8 in. wide

Ordering Information

Model	Description
6532	32-Channel 4-Input Digital Receiver VME Board, 16k FIFOs

Options:

-008	FPDP Inputs
-012	ECL diff. inputs
-023	32k FIFOs
-024	64k FIFOs
-035	Two comm ports on P2
-036	Four front panel C40 comm ports

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