Model 4283

Single TMS320C30 Processor MIX Baseboard

Features

- Accepts up to 3 MIX expansion modules
- 40 MFLOPS peak processing power
- 1, 4 or 8 MB dual-access memory
- 256 kB zero-wait-state CMOS static RAM supports high speed processing
- 128 kB EPROM with debug firmware

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TI Third Party Network Member DSP TEXAS INSTRUMENTS

Ordering Information

Model	Description
4283	Processor with 1 MB DRAM, 32 MHz clock
Options:	
-002	4 MB DRAM
-007	8 MB DRAM
-400	40 MHz clock

General Information

Serving as the basic platform on which to configure a custom VMEbus MIX subsystem, the Model 4283 incorporates the TMS320C30—one of the most powerful 32-bit floating-point DSPs—to act as a controller and perform high-speed signal processing. Although the Model 4283 has enough power to operate standalone in many applications, its speed and flexibility are enhanced by adding MIX modules.

Customized Data I/O

A wide variety of analog I/O MIX expansion modules are available to provide various speed, resolution and multichannel capabilities. A/D resolution can be as high as 18 bits at 200 kHz, or 12 bits at 10 MHz. Many modules provide D/A conversion for analog outputs. Other A/D converters provide up to 32 channels of simultaneous sample-and-hold. Adding serial or parallel digital I/O modules allows control and/or communication with other digital devices.

Flexible VMEbus Control

The Model 4283 has both master and slave VMEbus capabilities. As a bus master it can read from and write to the entire 32-bit address space of the VMEbus, thus accessing any external slave device. As a host controller it can also act as a bus arbiter for multiple bus masters. The Model 4283 can also generate and respond to interrupts.

Dual-Access RAM

A 1, 4 or 8 MB dual-access DRAM provides an extremely powerful structure for passing data and programs between the C30 and the VMEbus.

From the VMEbus, it appears as a relocatable slave memory in A24/A32 address space. From the C30, it is mapped directly onto the primary bus.

Specifications

Processor
TMS320C30, 32 or 40 MHz clock

Dual-Access RAM
Size: 1 MB (256k x 32), 4 MB (1M x 32), or 8 MB (2M x 32)
Arbitration: hardware, fully transparent
C30 access: memory-mapped on primary bus; three wait states
VME access: slave, relocatable on 1 MB boundaries; 260 ns DTACK delay

SRAM: 256 kB (64k x 32); memory-mapped on C30 primary bus, zero wait state

EPROM: 128 kB (32k x 32); memory-mapped on C30 primary bus, one wait state

Expansion bus: conforms to MIX standard with 32 bits for data and address

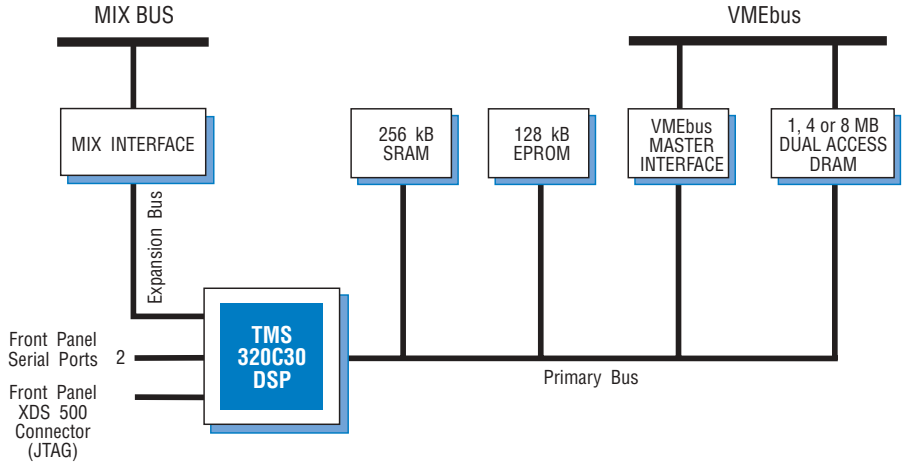
Connectors
XDS: 12-pin for TI XDS-500 Emulator;
I/O: 17-pin, front panel, for serial ports, timers, interrupts and flags

VMEbus Compliance
Master: D32 A32 I(1-7) IH(1-7)
Slave: D32 A32

Power: 2.4 A at +5 V dc

Size: standard 6U VMEbus board, single slot; board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 0.8 in. wide

Block Diagram, Model 4283



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