New!

Model 7853

4/2-Ch. DDC, four 200 MHz 16-bit A/Ds, Beamformer - x8 PCIe

Features

- Built-in Beamformer supports multiboard systems
- Programmable Power Meter and Threshold Detect per channel
- Four 200 MHz, 16-bit A/Ds
- 2 or 4 Channels of DDC
- PCI Express 2.0 (Gen. 2) interface up to x8 wide
- Independent 32-bit DDC tuning for all channels
- DDC decimation range from 2 to 256 or from 2 to 65536
- Independent decimation factors for each channel
- Default filters offer 0.2 dB ripple and 100 dB rejection
- LVPECL clock/sync bus for multiboard synchronization

General Information

Model 7853 is a high-speed software radio board designed for processing baseband RF or IF signals from a communications receiver. It features four 200 MHz 16-bit A/Ds supported by a high-performance 4-channel installed DDC (digital down-converter) and a complete set of beamforming functions. With buit-in multiboard synchronization, it is ideally matched to the requirements of real-time software radio and radar systems.

The 7853 attaches to motherboards with half-length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing.

DDC Input Selection and Tuning

The Model 7853 employs an advanced FPGA-based digital downconverter engine consisting of two or four DDC channels. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC channel. In this way, many different configurations can be achieved including one A/D driving all four DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the DDC channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

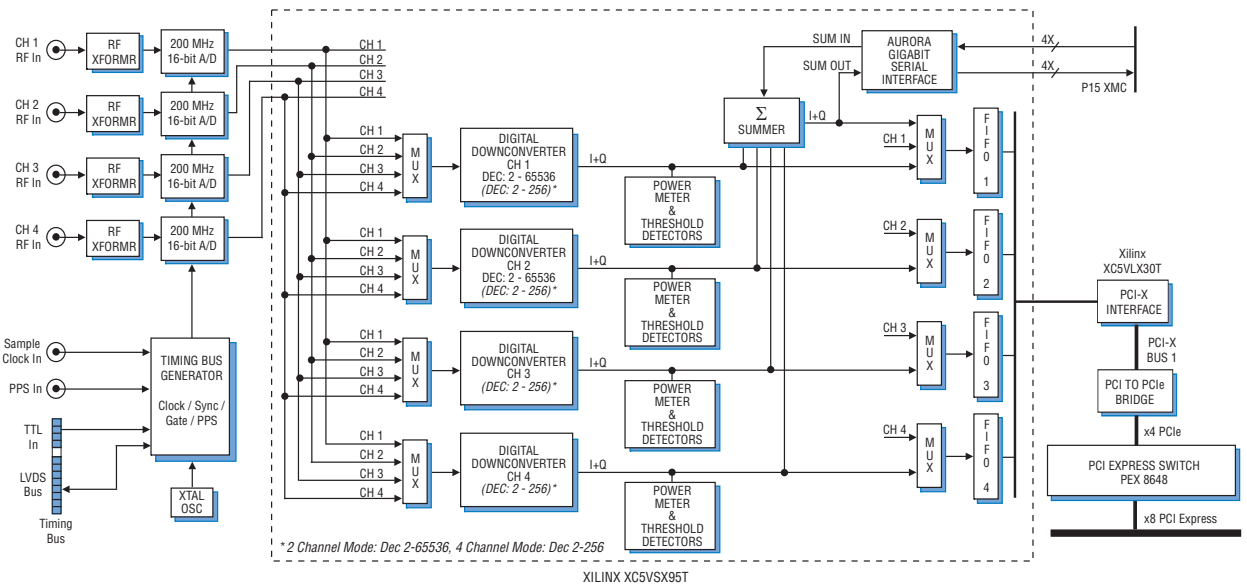
Decimation and Filtering

Each of the four DDC channels can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. The DDC core can be configured in four-channel mode with each channel offering decimations between 2 and 256, or in two-channel mode with each channel having a decimation range of 2 to 65536, for applications that require a wider range of decimations.

The decimating filter for each DDC channel accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N.

Power Meters

Each DDC includes a power meter that continuously measures the individual average power output. The power meters calculate and present average power measurements for each channel in easy-to-read registers. The time constant of the averaging interval for each meter is programmable up to 8 kilosamples. Threshold detectors can generate interrupts when the calculated power levels exceed or fall below user-programmable thresholds, ideal for scanning and monitoring applications. ➤



PENTEK
Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

XMC Interface

For large systems, multiple 7853's can be chained together via a built-in Xilinx Aurora interface through the P15 XMC connector.

This link creates a board-to-board summation expansion chain for creating larger multi-channel beamformer systems.

Xilinx's Aurora protocol is used to provide an efficient x4, 1.25 GB/sec point-to-point data path between boards.

➤ Beamformer

In addition to the A/Ds and DDCs, these Models include essential resources of a complete beamforming subsystem. First, each DDC channel provides user-programmable I & Q phase and gain adjustments to apply beamforming weights. Then, a summation block adds the four DDC output channels.

An additional programmable-gain stage compensates for summation bit growth. A power meter and threshold detect block is provided for the sum output. The sum output is then delivered to the Channel 1 FIFO for delivery through the PCI-X bus.

For larger systems, multiple Models can be chained together using a built-in Xilinx Aurora engine. It accepts an x4 gigabit sum input stream from a previous board and propagates an x4 sum output stream to the next board through the P15 XMC connector.

Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D data or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D data or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input rate and output rate to support different DDC decimation settings between the banks and efficient block transfers to the PCI bus.

Clocking and Synchronization

The Model 7853 architecture includes a flexible timing and synchronization circuit for the group of four A/D converters that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

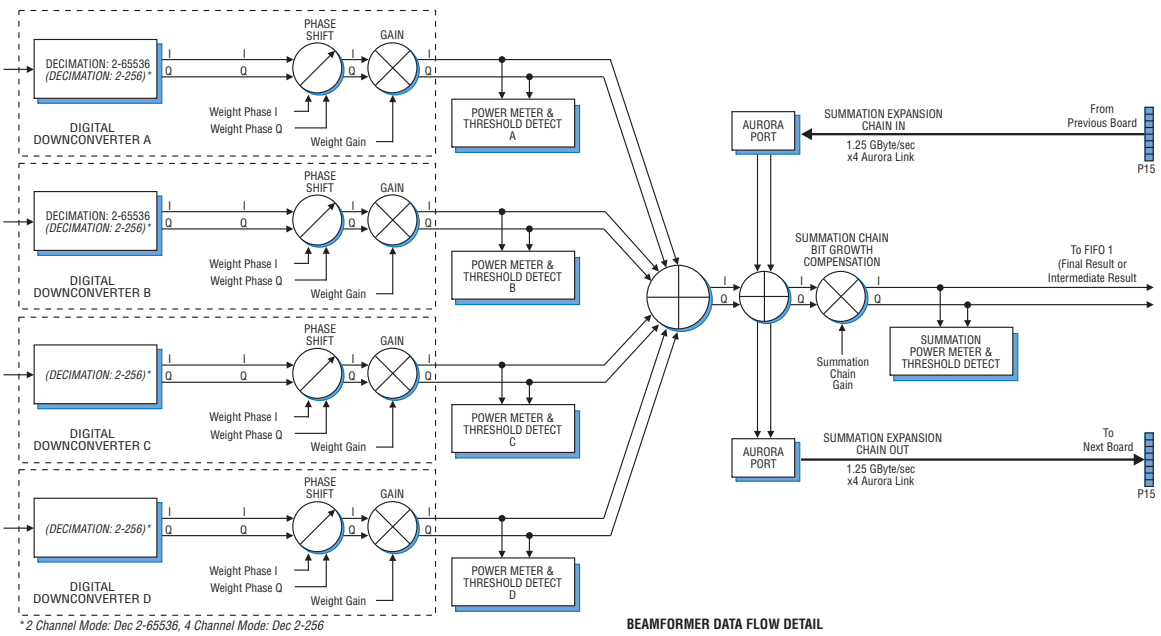
The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 7853's can be driven from each LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, many more boards can be synchronized with an external clock and sync generator.

PCI Express Interface

The 7853 includes a multiple port, 48-lane Gen. 2 PCI Express (PCIe) switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with one x4 connection provided to the 64-bit PCI-X interface.



*2 Channel Mode: Dec 2-65536, 4 Channel Mode: Dec 2-256

BEAMFORMER DATA FLOW DETAIL

PENTEK Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com www.pentek.com

Model 7853

4/2-Ch. DDC, four 200 MHz 16-bit A/Ds, Beamformer - x8 PCIe

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Internal Clock:** 200 MHz crystal osc.
- **External Clock:** 10 to 200 MHz
- **Resolution:** 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillator, external reference or LVPECL clocks

External Clock
- **Type:** Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled 50 ohms
- **Sync/Gate Bus:** 26-pin connector, clock/sync/gate/PPS, input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Digital Downconverter
- **Type:** IP core for Xilinx Virtex-5
- **Qty of DDC Channels:** 2 or 4
- **Center Frequency Tuning:** 4 tuning words, one for each DDC channel
- **Center Frequency Tuning Range:** DC to f_s with 32 bit resolution
- **NCO SFDR:** –120 dBFS
- **Channel Phase Offset Adjustment:** 32-bit resolution
- **Channel Gain Adjustment:** 32-bit resolution
- **Input Selection for DDC Banks:** Any channel can select any of the four A/Ds
- **Decimation Range (N):**
  - **2-Channel Mode:** 2 to 65536
  - **4-Channel Mode:** 2 to 256
- **FIR Filter:** Default passband $0.8*f_s/N$ with 0.2 dB passband ripple and 100 dB adjacent channel rejection
- **FIR Filter Coefficients:** 18 bits, user-programmable (default values provided)
- **Qty FIR Filter Taps:** 28*N/8
- **Output Format:** 24 bits I + 24 bits Q
- **Output Spectrum Modes:** Normal or frequency-reversed
- **Output Spectrum Offset:** No offset or offset by one-half the output bandwidth

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Output Multiplexer and FIFO
- **Qty Output FIFOs:** Four
- **FIFO Source Selection:** Independent multiplexer selects DDC output or A/D

PCI to PCIe Interface
- **PCI-X Bus:** 64 bits, 100 MHz and 64 or 32 bits at 33 or 66 MHz
- **DMA:** 4-channel demand-mode and chaining controller
- **PCIe Interface:** Gen. 2, x8 width
- **PCIe Ports:** one x4 port to PCI-X bus one x8 port to PCIe motherboard

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in.

Ordering Information

Model	Description
7853	4-Channel DDC with four 200 MHz, 16-bit A/Ds and Beamformer - Half-length x8 PCIe
Options:	
-731	Two-slot heat sink

Contact Pentek for additional available options.

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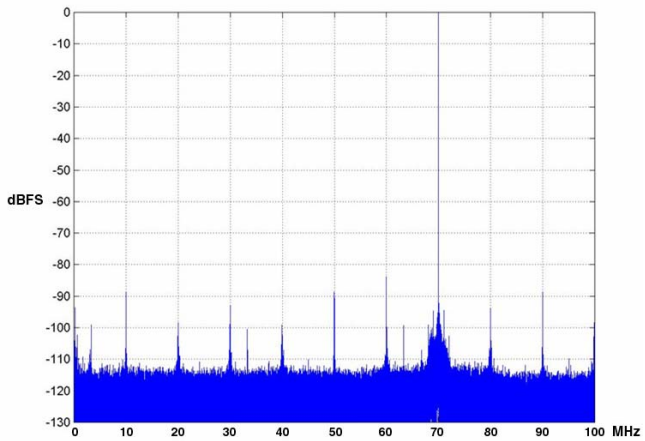
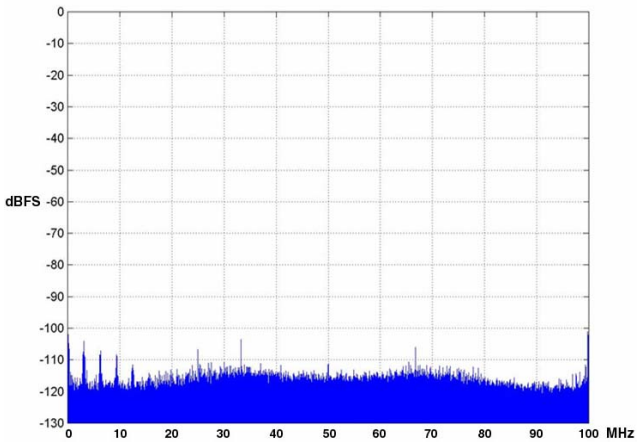
A/D Performance

Spurious-Free Dynamic Range



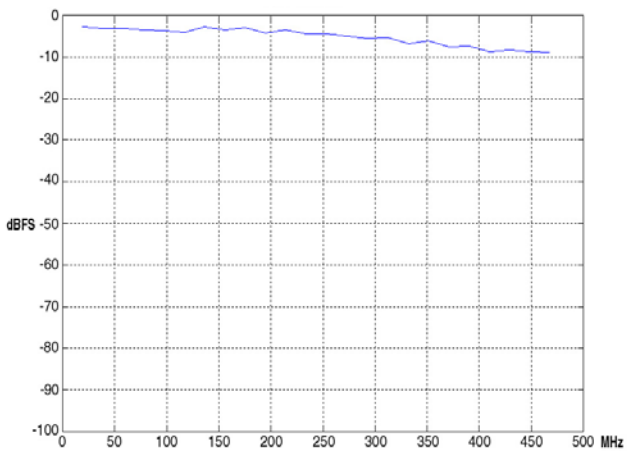
f_{in}= 70 MHz, f_s= 200 MHz, Internal Clock

Spurious Pickup



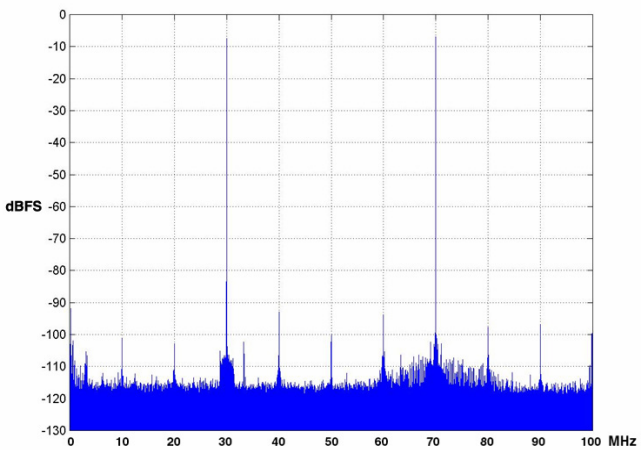
f_s= 200 MHz, Internal Clock

Input Frequency Response



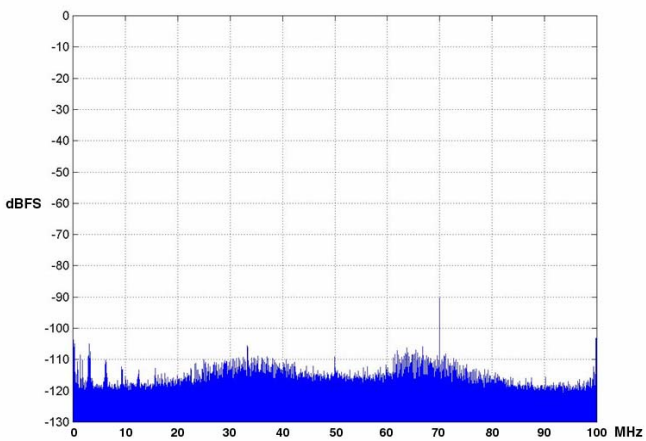
f_s= 200 MHz, Int. Clock

Two-Tone SFDR



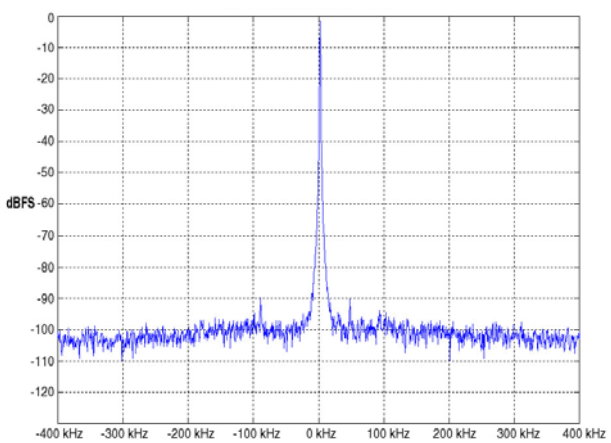
f_{in1}= 30 MHz, f_{in2}= 70 MHz, f_s= 200 MHz, Int. Clock

Adjacent Channel Crosstalk



f_{in}= 70 MHz, A_{in}= 0 dBFS, f_s= 200 MHz, Int. Clock

Phase Noise at 70 MHz



f_s= 200 MHz, Int. Clock