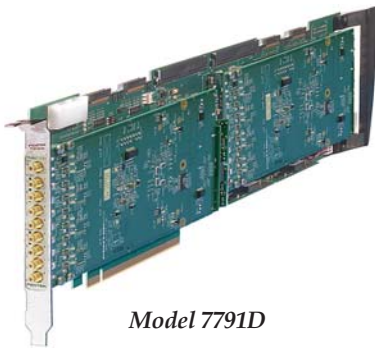


New!

Models 7791, 7791D

Programmable Multifrequency Clock Synthesizers - x16 PCIe



Model 7791D

Features

- Simultaneous synthesis of five or ten different clocks
- Eight or 16 SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: -105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four or eight programmable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCIe bus interface

General Information

These Models generate up to 16 synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. Model 7791 generates eight clocks while Model 7791D generates sixteen.

Clock Synthesizer Circuits

These Models use the Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO (Voltage Controlled Crystal Oscillator) to provide the base frequency for the clock synthesizer. Each of the VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The CDC7005's can output up to five frequencies each. These Models can be programmed to route any of these 20 or 40 frequencies to the board's output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight or 16 front panel SMC connectors supply synthesized clock outputs driven from the five or ten clock output drivers, as shown in the block diagram. This supports a single identical clock to all outputs or up to 16 different clocks to various outputs.

With independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a

wide range of clock configurations is possible. In systems where more than ten different clock outputs are required simultaneously, multiple 7791D's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Express Interface

These Models include a multiple port, 48-lane Gen. 2 PCIe switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface.

Specifications

Front Panel Reference Input

Connector Type: SMC

Input Impedance: 50 ohms

Reference Frequency: 5 to 100 MHz

Input Level: -6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners

Quantity: Four or eight

Type: Texas Instruments CDC7005

Frequency Dividers: 1, 2, 4, 8 and 16

Programmable VCXOs (Quantity: 4 or 8)

Frequency Range: 50 to 700 MHz

Tuning Resolution: 32 bits

Unlocked Accuracy: ±20 ppm

Front Panel Clock Outputs (Quantity: 8 or 16)

Connector Type: SMC

Output Impedance: 50 ohms

Output Level: +3 dBm @ 700 MHz

Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI to PCIe Interface

PCIe Interface: Gen. 2, x16 width

PCIe Ports: one x4 port to PCI bus, one x16 port to PCIe motherboard

Operation: control and status interface

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Full-length PCIe, 4.38 in. x 12.3 in.



Ordering Information

Model	Description
7791	Programmable Multifrequency Clock Synthesizer - Full-length x16 PCIe
7791D	Dual Programmable Multifrequency Clock Synthesizer - Full-length x16 PCIe

