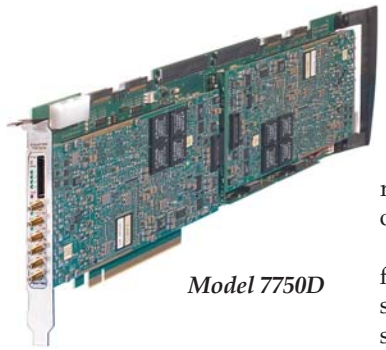
Quad/Octal 200 MHz, 16-bit A/D with Virtex-5 FPGAs - x16 PCIe



Model 7750D

GateFlow ReadyFlow Board Support Package

Features

- Complete software radio interface solution
- PCI Express 2.0 (Gen. 2) Interface up to x16 wide
- Four or eight 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR2 SDRAM
- Two or Four Xilinx Virtex-5 FPGAs
- Up to 5.12 seconds of data capture at 200 MHz
- LVPECL clock/sync bus for multimodule synchronization
- Up to 64 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Model 7750 is a high-speed data converter suitable for connection as the HF or IF input of a communications system. It features either four 200 MHz, 16-bit A/Ds (Model 7750) or eight A/Ds (Model 7750D). These are supported by an array of data processing and transport resources ideally matched to requirements of high-performance systems.

The 7750 attaches to motherboards with full length PCI Express (PCIe) interface slots for installation in various PCs, blade servers and computer systems.

A/D Converter Stage

The front end accepts four or eight full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-5 FPGA for signal processing or for routing to other module resources.

Virtex-5 FPGAs

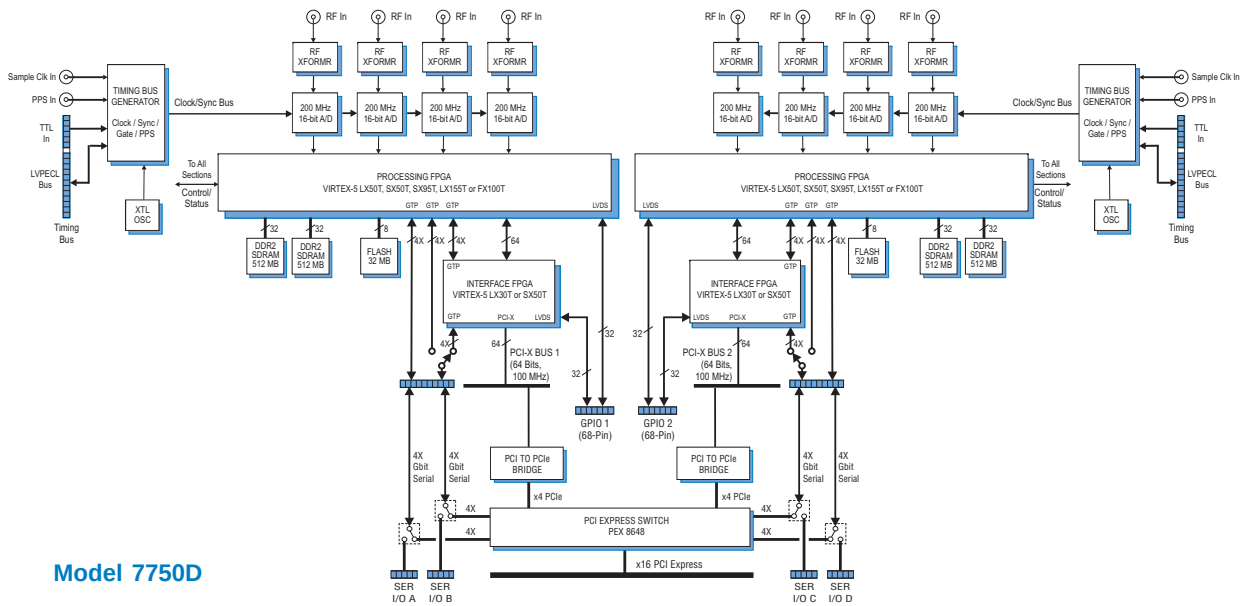
The Model 7750 architecture includes two (Model 7750) or four (Model 7750D) Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering, and SDRAM memory control. In addition, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user- created IP with the factory-shipped functions.

There are two FPGA types on the 7750: processing and interface. The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, interface FPGA, programmable LVPECL I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T and FX100T.

The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, these Models can be optionally configured with an LX155T in the processing FPGA position for 155,648 logic cells.

The interface FPGA provides board connections including PCI-X or PCI Express. Implementing the PCI interfaces in this FPGA keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E Slices.

Option -104 installs a GPIO connector with 16 pairs of LVDS connections to each processing FPGA, and 16 pairs of LVDS connections to each interface FPGA for custom I/O. ➤



Model 7750D

PENTEK

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Quad/Octal 200 MHz, 16-bit A/D with Virtex-5 FPGAs - x16 PCIe

Clocking and Synchronization

The Model 7750 architecture includes a flexible timing and synchronization circuit for each bank of four A/D converters, allowing the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

Each timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

One or two front panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 7750s can be driven from each LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More bords can be synchronized with an external clock and sync generator.

Memory Resources

Up to two independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. Each memory bank can be easily accessed through the PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI Express Interface

The 7750 includes a multiple port, 48-lane Gen 2 PCI Express (PCIe) switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface, allowing high-speed data transfers to and from the motherboard. Switch ports each include buffer memory to minimize bottlenecks, with two x4 PCIe connections provided to each FPGA, as well as one x4 connection to each 64-bit PCI-X interface.

Option -5xx adds two full duplex 4X gigabit serial paths on high-speed connectors, supporting PCIe or other gigabit protocols.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Internal Clock:** 200 MHz crystal osc.
- **External Clock:** 10 to 200 MHz
- **Resolution:** 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock
- **Type:** Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms
- **Sync/Gate Bus:** 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array
- **Processing FPGA:** Xilinx Virtex-5 XC5VSX50T (one for 7750, two for 7750D); optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VLX155T and XC5VFX100T
- **Interface FPGA:** Xilinx Virtex-5 XC5VLX30T (one for 7750, two for 7750D); optional FPGA: XC5VSX50T

Custom I/O
- **Available only with SX95T, LX155T and FX100T FPGAs**
- **Option -104:** Provides GPIO with 16 LVDS pairs to each processing FPGA and 16 pairs to each interface FPGA

Memory
- **DDR2 SDRAM:** Up to 1 GB in two banks per processing FPGA (2 GB max.)

PCI to PCIe Interface
- **PCI-X Bus:** 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz
- **DMA:** 4 channel demand-mode and chaining controller per PCI bus
- **PCIe Interface:** Gen. 2, x16 width
- **PCIe Ports:** two x4 ports per FPGA
  - one x4 port per PCI bus
  - one x16 port to PCIe motherboard

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Full-length PCIe , 4.38 in. x 12.3 in.

Ordering Information

Model	Description
7750	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Full-length x16 PCIe
7750D	Octal 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Full-length x16 PCIe
Options:	
-104	FPGA I/O through the GPIO connector(s)
-5xx	Gigabit Serial I/O - two full duplex 4X paths (Model 7750) or four full duplex 4X paths (Model 7750D)

Contact Pentek for additional available options.

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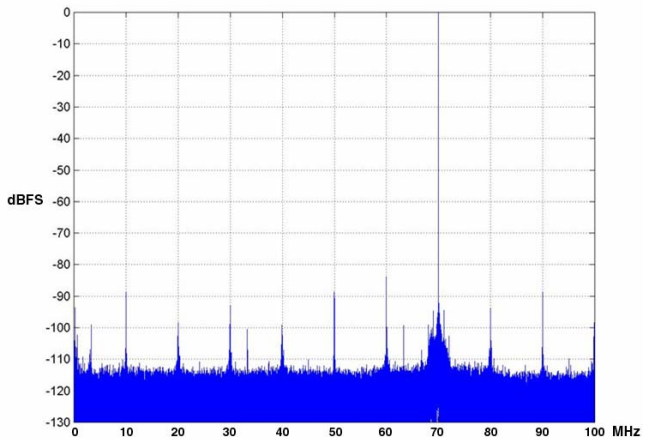
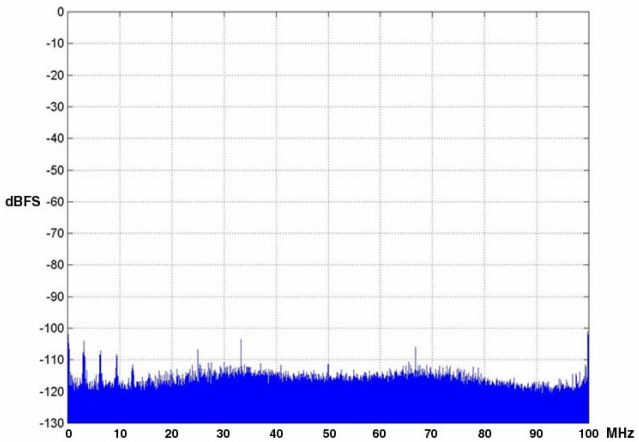
A/D Performance

Spurious-Free Dynamic Range



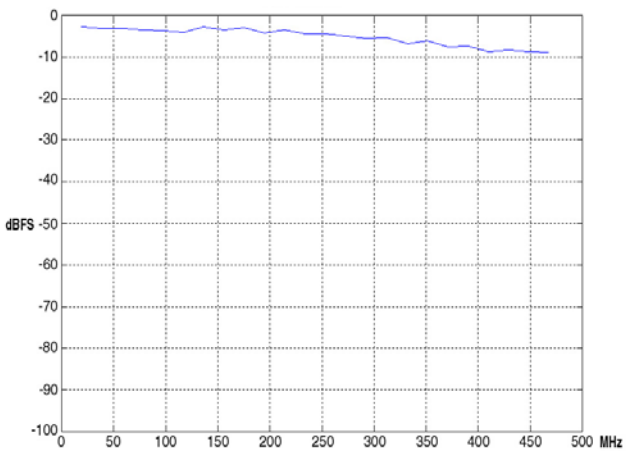
f_{in}= 70 MHz, f_s= 200 MHz, Internal Clock

Spurious Pickup



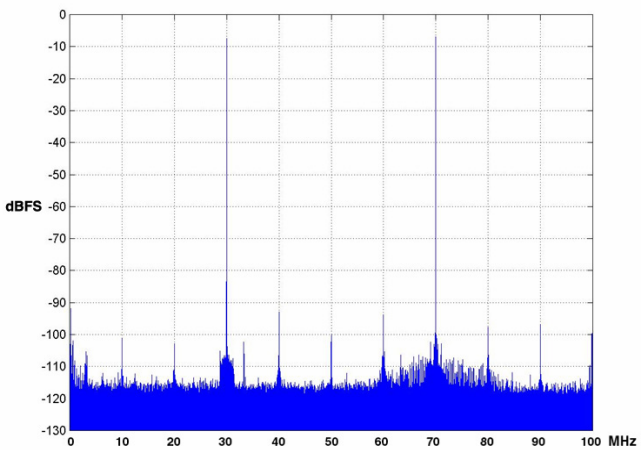
f_s= 200 MHz, Internal Clock

Input Frequency Response



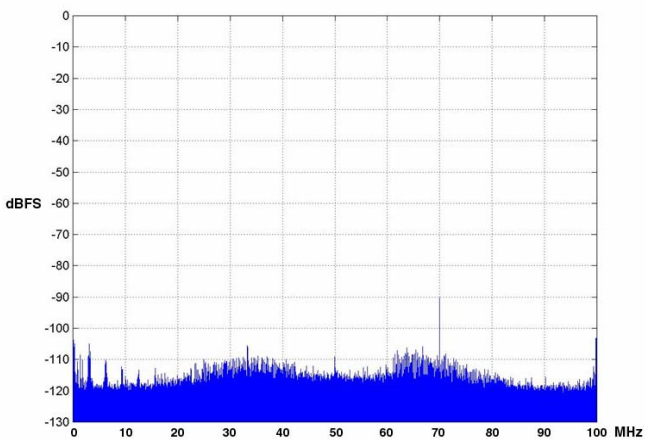
f_s= 200 MHz, Int. Clock

Two-Tone SFDR



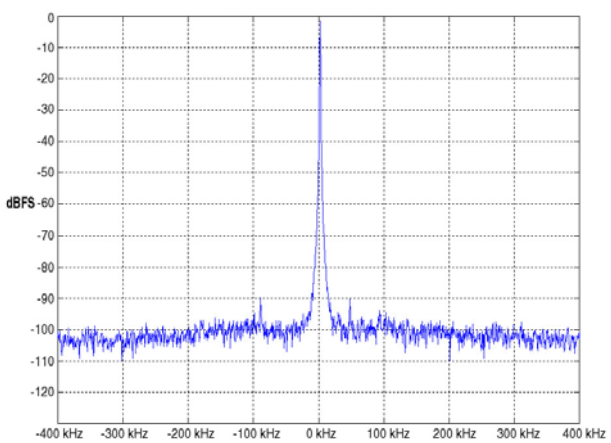
f_{in1}= 30 MHz, f_{in2}= 70 MHz, f_s= 200 MHz, Int. Clock

Adjacent Channel Crosstalk



f_{in}= 70 MHz, A_{in}= 0 dBFS, f_s= 200 MHz, Int. Clock

Phase Noise at 70 MHz



f_s= 200 MHz, Int. Clock