Model 7690





Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: -105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four quad VCXOs allow selection from 16 different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface



Ordering Information

Model Description

7690 Multifrequency Clock Synthesizer - PCI

Options

Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz

* Contact Pentek to order specific frequencies



General Information

Model 7690 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7690 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7690 can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independent quadVCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide

range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7690's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface

The Model 7690 uses an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. It attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

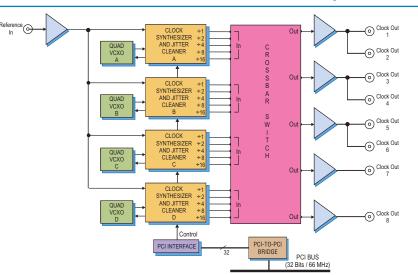
Specifications

Front Panel Reference Input Connector Type: SMC Input Impedance: 50 ohms **Reference Frequency:** 5 to 100 MHz Input Level: -6 dBm to +10 dBm PLL Clock Synthesizers & Jitter Cleaners Quantity: Four **Type:** Texas Instruments CDC7005 Frequency Dividers: 1, 2, 4, 8 and 16 Quad VCXOs (Quantity: 4) Frequencies per VCXO: 4*, softwareprogrammable Frequency Range: 50 to 700 MHz Unlocked Accuracy: ±20 ppm Front Panel Clock Outputs (Quantity: Eight) **Connector Type: SMC** Output Impedance: 50 ohms Output Level: +3 dBm @ 700 MHz Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface

PCI Bus: 32-bit, 66 MHz (supports 33 MHz) Operation: control and status interface Environmental

Operating Temp: 0° to 50° C **Storage Temp:** –20° to 90° C **Relative Humidity:** 0 to 95%, non-cond. **Size:** Standard half-length PCI board



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