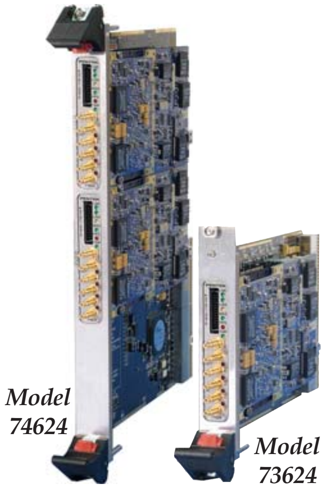
New!

Models 72624 73624 and 74624

2- or 4-Channel, 34- or 68-Signal Adaptive IF Relay - cPCI



Cobalt

Features

- Modifies 34 or 68 IF signals between input and output
- Up to 80 MHz IF bandwidth
- Two/four 200 MHz 16-bit A/Ds
- Two/four 800 MHz 16-bit D/As
- 34/68 DDCs and 34/68 DUCs (digital downconverters and digital upconverters)
- Signal drop/add/replace
- Frequency shifting and hopping
- Amplitude boost and attenuation
- PCI-X system interface

General Information

Models 72624, 73624 and 74624 are members of the Cobalt® family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71624 XMC modules mounted on a cPCI carrier board. Model 72624 is a 6U cPCI board while the Model 73624 is a 3U cPCI board; both are equipped with one Model 71624 XMC. Model 74624 is a 6U cPCI board with two XMC modules rather than one.

As IF relays, they accept two or four IF analog input channels, modify up to 34 or 68 signals, and then deliver them to two or four analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the board

These models support many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board's data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay.

A PCI-X system interface supports control, status and data transfers.

Adaptive Relay Input Overview

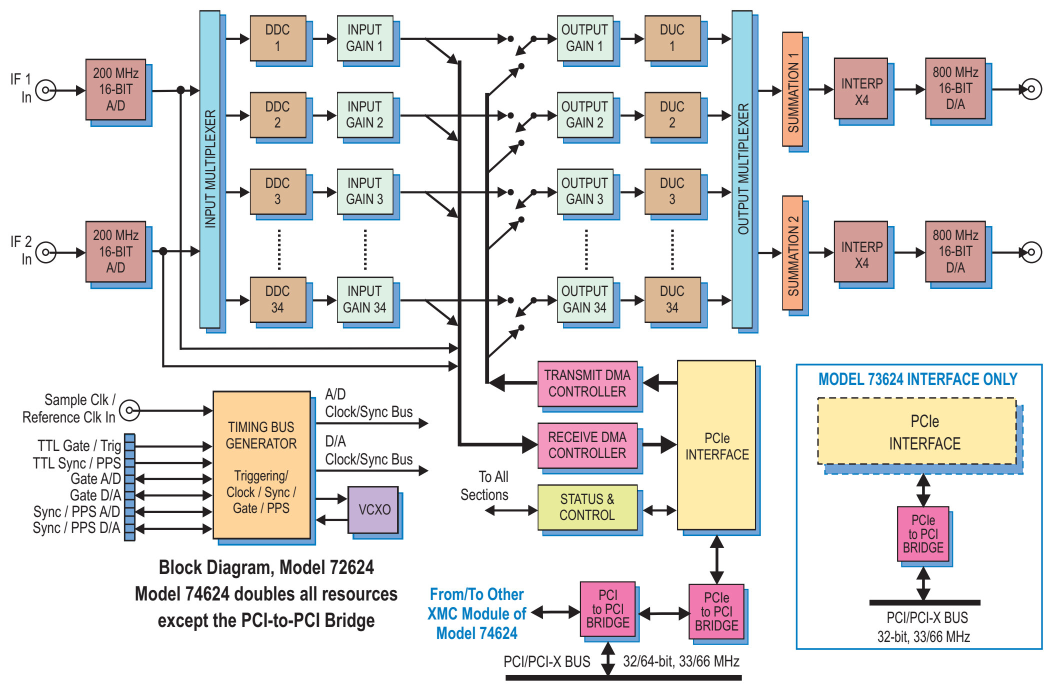
These models digitize two or four analog IF inputs using 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 or 68 DDCs (digital downconverters) can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of two A/Ds.

Baseband I+Q DDC outputs are scaled in a programmable gain/attenuation block before being delivered across the PCI-X system interface to target memory, typically associated with a system processor. Here, the signals can be analyzed, classified, demodulated, decrypted or decoded, depending on the application.

Samples from each A/D converter can also be delivered across PCI-X to system memory so that the processor can access wideband IF data. By performing an FFT, the processor can identify signals and then tune the DDCs accordingly.

Adaptive Relay Output Overview

The output stage of these models consists of 34 or 68 DUCs (digital upconverters) and two or four 800 MHz 16-bit D/A converters. Each DUC accepts baseband I+Q ➤



Block Diagram, Model 72624
Model 74624 doubles all resources except the PCI-to-PCI Bridge

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➤ signals from either the local DDCs or from system memory.

DUC inputs are scaled in programmable gain/attenuation blocks similar to those in the input stages. Each DUC is independently programmable for data source selection (DDC or memory), upconvert tuning frequency and bandwidth (interpolation).

The translated DUC outputs are directed to either of two or four summation blocks, each associated with one of the two or four D/A converters using a final interpolation factor of x4. After conversion, the IF analog outputs of each D/A can contain signals from any combination of the 34 or 68 DUCs.

Xilinx Virtex-6 FPGA

The SX315T Virtex-6 FPGA with 1344 DSP48E engines is well suited for the demanding signal processing tasks required by the adaptive relay of these models. Because of the complexity and proprietary nature of these functions, the FPGAs cannot be extended or modified by the user.

A/D Converters

The front-end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two or four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into one or two Virtex-6 FPGAs for the data capture and all of the remaining adaptive relay signal processing operations.

Digital Downconverters

Each of the FPGA-based DDCs has an independent mixer and local oscillator with a 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency, nominally 200 MHz. An IF input signal can be downconverted to a complex (I+Q) signal centered at 0 Hz by setting the DDC tuning frequency to its center frequency.

The DDC output bandwidth is determined by its decimation setting, which is programmable from 512 to 8192 in steps of 8. Each DDC can have a different decimation, thereby supporting up to 34 or 68 different signal bandwidths.

The fixed 80% decimating output filters deliver an output bandwidth equal to $0.8*f_s/N$, where N is the decimation setting and f_s is the A/D sample rate. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

Input Gain Blocks

Each DDC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each input gain block, which is a complex digital multiplier, accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Receive DMA Controllers

Two or four output DMA engines deliver data across the PCI-X interface into user-specified memory locations in PCI-X target memory. DMA engine #1 can deliver either raw samples from A/D Ch 1 or channel-interleaved 24-bit I and Q baseband samples from the 34 DDCs of the first XMC module. Data samples from each DDC can be independently enabled/disabled for output. DMA engine #2 can deliver raw samples from A/D Ch 2. This sequence repeats for the second XMC module of Model 74624.

When a target memory buffer is filled, these models issue an interrupt to the system processor and then begin filling an alternate buffer. In this way, the processor is always informed when and where data is available for retrieval. Packet headers identify the DDC and show the number of subsequent data samples.

Transmit DMA Controller

Each of the FPGA-based 34 or 68 DUCs interpolates complex (I+Q) baseband signals and translates them to the desired IF output center frequency.

The data source for each DUC can be independently selected from its corresponding DDC output, or from PCI-X target memory buffers fetched by the transmit DMA controller, where header information steers the memory data to the appropriate DUC channel.

Like the receive DMA controllers, once a data buffer is emptied, these models signal the processor with an interrupt and move to the next assigned buffer to continue fetching data.

Output Gain Blocks

The complex baseband input for each DUC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated.

Each of the output gain blocks accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB. ➤

➤ Digital Upconverters

The interpolation filter increases the baseband input sample rate by an interpolation factor typically equal to the decimation factor of the corresponding DDC. This interpolation factor is programmable from 512 to 8192 in steps of 8. Using this strategy, the interpolation sample rate equals the A/D sample rate, nominally 200 MHz.

A complex digital mixer upconverts the interpolated baseband signal to the desired IF output center frequency. This frequency is determined by a local oscillator programmable with a 32-bit integer from DC to f_s, where f_s is the interpolator output frequency, nominally 200 MHz.

Each of the DUCs can have an independent interpolation factor and tuning frequency. However, all DUC outputs sharing a common summation block must have the same sample rate.

Summation Blocks

Two or four summation blocks accept any combination of the upconverted DUC signals by setting an enable bit for each DUC's contribution. Each DUC output can be enabled for none, one or both of the summation blocks.

The summation blocks deliver only real output samples to the subsequent D/A converter stage.

D/A Converters

One or two TI DAC5688 dual-channel D/As accept the summed upconverted data streams, one from each summation block, and operate in their non-translating dual, real baseband mode. Their built-in interpolation filter is typically set to x4 mode, boosting the summation output sample rate from a nominal 200 MHz to 800 MHz. This simplifies the output low pass reconstruction filtering requirements.

Two or four transformer-coupled analog IF outputs are delivered through one or two pairs of front panel SSMC connectors.

Clocking and Synchronization

Two or four internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from one or two on-board programmable VCXOs (voltage-controlled crystal oscillators). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the internal oscillator.

One or two front panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73624: 32 bits only.

Form Factor Adaptors

All Pentek Cobalt XMC modules can be adapted to other standard embedded system form factors through the use of adaptor boards. Available versions include PCIe, 3U and 6U OpenVPX, 3U and 6U cPCI, and AMC. For more information and the Pentek's Product Selector Tool visit our website at: www.pentek.com. ➤

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2- or 4-Channel, 34- or 68-Signal Adaptive IF Relay - cPCI

➤ Specifications

Models 72624 & 73624: 2 A/Ds, 34 DDCs, 34 DUCs, 2 D/As

Model 74624: 4 A/Ds, 68 DDCs, 68 DUCs, 4 D/As

Front Panel Analog Signal Inputs (2 or 4)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Quantity:** 2 or 4
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** 34 or 68
- **Decimation Range:** 512 to 8192, in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >100 dB
- **Phase Offset:** 1 bit, 0 or 180 degrees
- **FIR Filter:** 18-bit coefficients
- **Output:** Complex, 16-bit I + 16-bit Q
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Input Gain Blocks
- **Quantity:** 34 or 68
- **Data**: Complex, 16-bit I + 16-bit Q
- **Gain Range:** 16-bit Q8.8 format, approximately +/–48 dB

Output Gain Blocks
- **Quantity:** 34 or 68
- **Data**: Complex, 16-bit I + 16-bit Q
- **Gain Range:** 16-bit Q8.8 format, approximately +/–48 dB

Digital Upconverters
- **Quantity:** 34 or 68
- **Interpolation Range:** 512 to 8192, in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **FIR Filter:** 18-bit coefficients, 16-bit output
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Analog Output Channels:** 2 or 4
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 200 MHz max.
- **Output Signal:** Real
- **Output Sampling Rate:** 800 MHz max. with 4x interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs (2 or 4)
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: (1 or 2)
- On-board clock synthesizers generate two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connectors, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accept 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2)
- **Type:** 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
- **Required:** Xilinx Virtex-6 XC6VSX315T

PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz Model 73624: 32 bits only

Environmental
- **Standard:**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-cond.
- **Option 702 L2 Extended Temp (air-cooled):**
  - **Operating Temp:** -20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-cond.
- **Option 712 L2 Extended Temp (conduction-cooled):**
  - **Operating Temp:** -20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board ➤

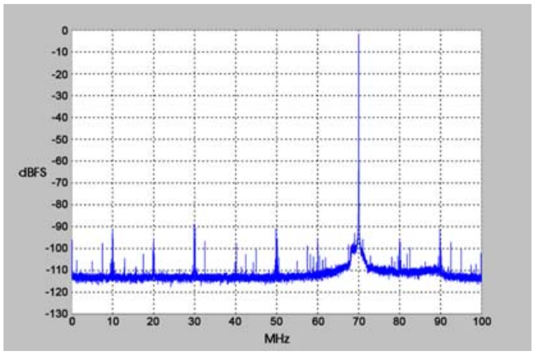
Ordering Information

Model	Description
72624	Dual-Channel 34-Signal Adaptive IF Relay - 6U cPCI
73624	Dual-Channel 34-Signal Adaptive IF Relay - 3U cPCI
74624	Quad-Channel 68-Signal Adaptive IF Relay - 6U cPCI
Options:	
-064	XC6VSX315T (required)
-702	L2 (air cooled) environmental level
-712	L2 (conduction cooled) environmental level
-730	2-slot heatsink

Contact Pentek for availability of rugged and conduction-cooled versions

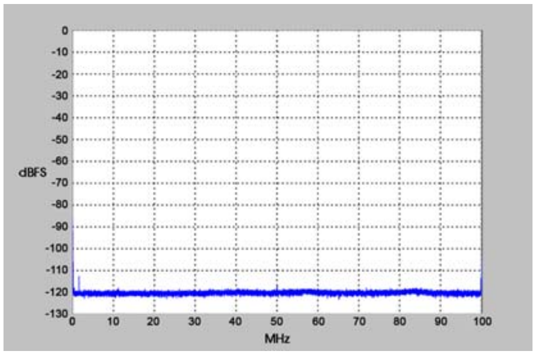
A/D Performance

Spurious Free Dynamic Range



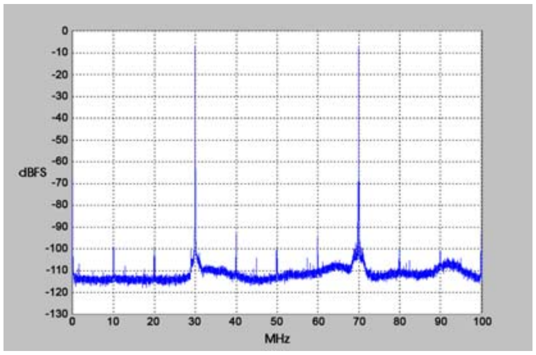
f_{in} = 70 MHz, f_s = 200 MHz, Internal Clock

Spurious Pick-up



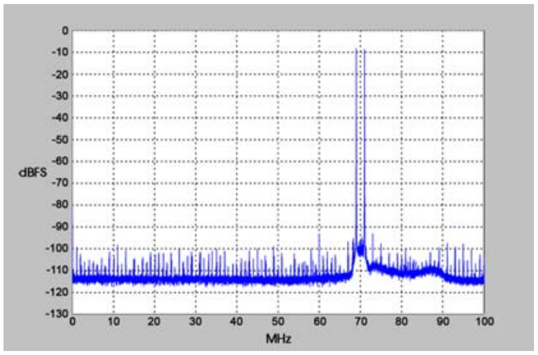
f_s = 200 MHz, Internal Clock

Two-Tone SFDR



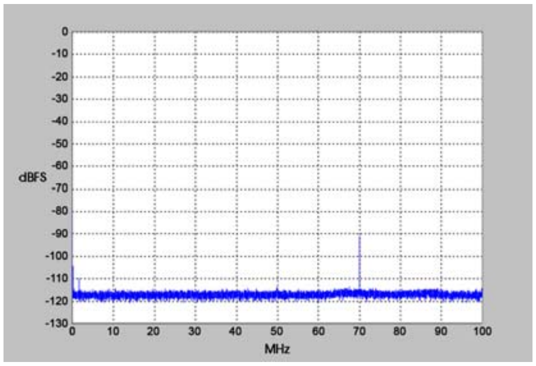
f_1 = 30 MHz, f_2 = 70 MHz, f_s = 200 MHz

Two-Tone SFDR



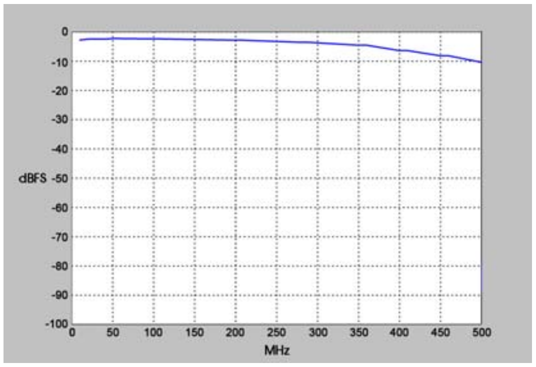
f_1 = 69 MHz, f_2 = 71 MHz, f_s = 200 MHz

Adjacent Channel Crosstalk Crosstalk



$f_{in\ Ch2}$ = 70 MHz, f_s = 200 MHz, Ch 1 shown

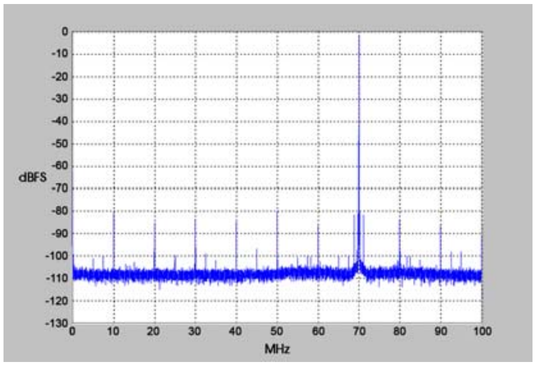
Input Frequency Response



f_s = 200 MHz, Internal Clock

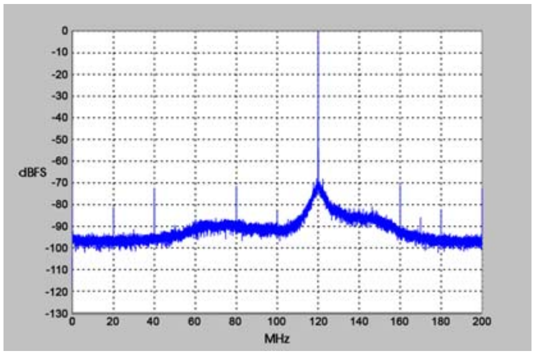
D/A Performance

Spurious Free Dynamic Range



f_{out} = 70 MHz, f_s = 200 MHz, Internal Clock

Spurious Free Dynamic Range



f_{out} = 140 MHz, f_s = 400 MHz, External Clock