Model 71771

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-7 FPGA - XMC

General Information

Model 71771 is a member of the Onyx™ family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As with a wide range of programmable interpolation factors, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71771 includes optional general-purpose and gigabit serial connectors for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71771 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71771 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

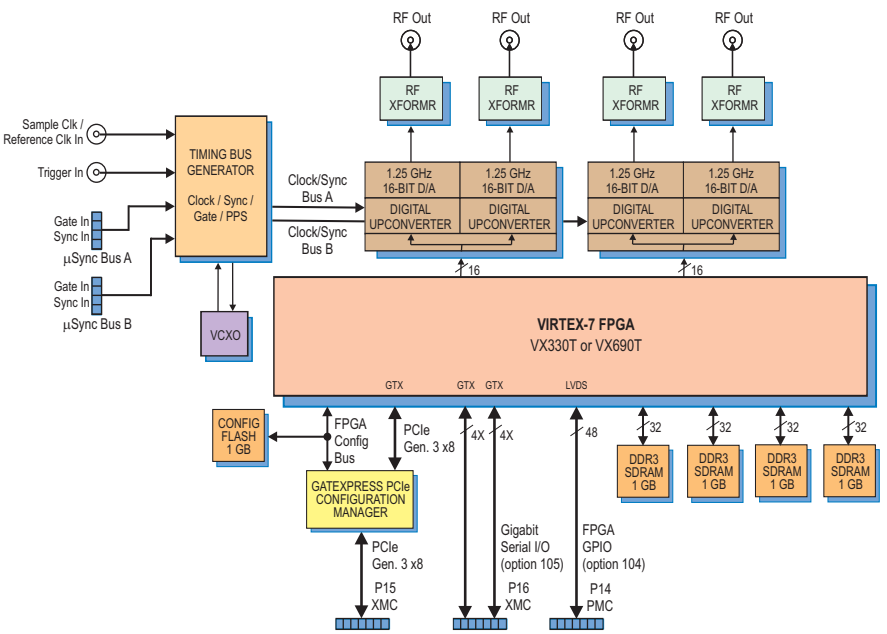
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Extended interpolation range from 2x to 1,048,576x
- Programmable output levels
- 250 MHz max. output bandwidth
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O



Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

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➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

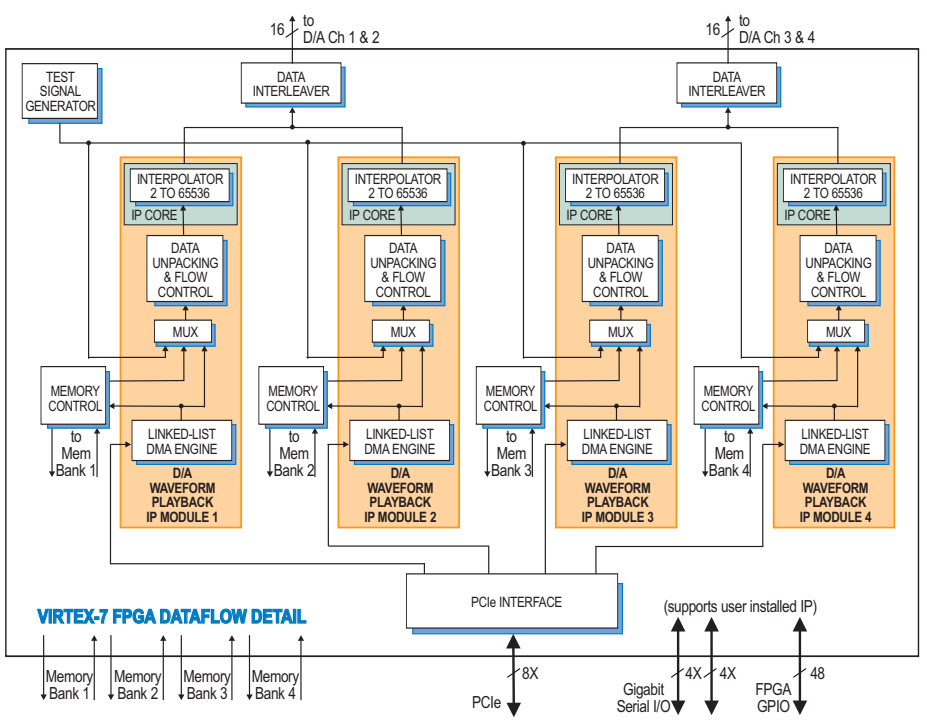
If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, the 71771 features an FPGA-based interpolation engine which adds two additonal interpolation stages programmable from 2x to 256x. The combined interpolation results ➤

D/A Waveform Playback IP Module

The Model 71771 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4. Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
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XMC Interface

The Model 71771 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71771 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model	Description
71771	4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-7 FPGA - XMC
Options:	
-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O through P14 connector
-105	Gigabit serial FPGA I/O through P16 connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8266	PC Development System See 8266 Datasheet for Options

➤ in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog output is through four front panel SSMC connectors. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly or can be divided by a built-in clock synthesizer circuit to provide different D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A pair of front panel µSync connectors allows multiple modules to be synchronized. In the slave mode, they accept CML inputs that drive the board's clock, sync and gate signals. In the master mode, the µSync connectors can drive the front panel timing signals for synchronizing a slave 71771 module. For larger systems, the Pentek Model 7192 High-Speed Synchronizer can drive multiple 71771's enabling large, multichannel synchronous configurations.

Memory Resources

The 71770 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 1 GB deep and is an integral part of the module's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers. In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 71771 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers.

Specifications

D/A Converters
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Front Panel Analog Signal Outputs
- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO, front panel external clock or µSync timing buses
- **Synchronization:** Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus: 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8 Gen. 3 available only with the VX330T-2 and VX690T-2 FPGAs

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

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