

New!

Model 7153

4/2-Ch. DDC, four 200 MHz 16-bit A/Ds, Beamformer - PMC/XMC



Features

- Built-in Beamformer supports multiboard systems
- Programmable Power Meter and Threshold Detect per channel
- Four 200 MHz, 16-bit A/Ds
- 2 or 4 Channels of DDC
- Independent 32-bit DDC tuning for all channels
- DDC decimation range from 2 to 256 or from 2 to 65536
- Independent decimation factors for each channel
- Default filters offer 0.2 dB ripple and 100 dB rejection
- LVPECL clock/sync bus for multimodule synchronization

General Information

Model 7153 is a 4-channel, high-speed software radio module designed for processing baseband RF or IF signals. It features four 200 MHz 16-bit A/Ds supported by a high-performance 4-channel DDC (digital downconverter) and a complete set of beamforming functions. With built-in multiboard synchronization, it is ideally matched to the requirements of real-time software radio and radar systems.

Model 7153 uses the industry standard PMC daughtercard format compatible with numerous carrier boards for VME, PCI, and CompactPCI.

A/D Converter Stage

The front end accepts four full scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling to four Texas Instruments ADS5485 200 MHz, 16-bit A/Ds.

The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing operations.

DDC Input Selection and Tuning

The Model 7153 employs an advanced FPGA-based digital downconverter engine consisting of two or four DDC channels. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC channel. In this way, many different configurations can be achieved including one A/D driving all four DDC channels and each of the four A/Ds driving its own DDC bank.

Each of the DDC channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sampling frequency.

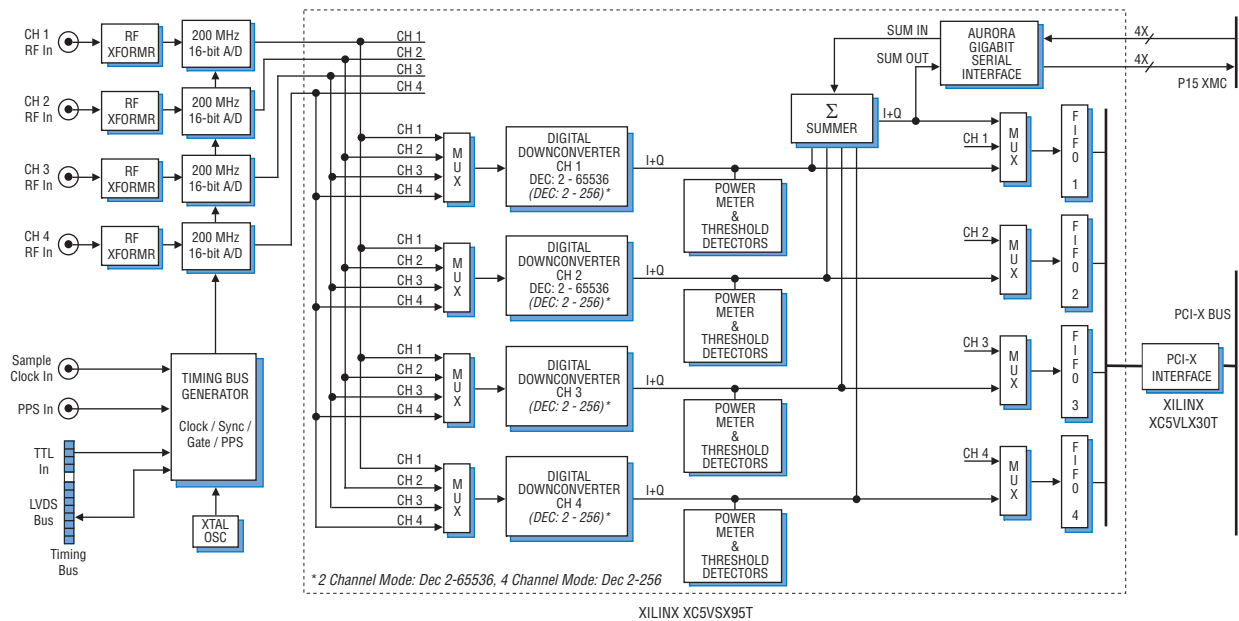
Decimation and Filtering

Each of the four DDC channels can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. The DDC core can be configured in four-channel mode with each channel offering decimations between 2 and 256, or in two-channel mode with each channel having a decimation range of 2 to 65536, for applications that require a wider range of decimations.

The decimating filter for each DDC channel accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N .

Power Meters

Each DDC includes a power meter that continuously measures the individual average power output. The power meters calculate and present average power measurements for each channel in easy-to-read registers. The time constant of the averaging interval for each meter is programmable up to 8 kilosamples. Threshold detectors can generate interrupts when the calculated power levels exceed or fall below user-programmable thresholds, ideal for scanning and monitoring applications. ➤



XMC Interface

The Model 7153 complies with the VITA 42.0 XMC specification. This standard provides serial data links between the XMC module and the carrier board. The 7153 beamformer architecture uses this link to create a board-to-board summation expansion chain for creating larger multichannel beamformer systems.

Xilinx's Aurora protocol is used to provide an efficient x4, 1.25 GB/sec point-to-point data path between boards.

► Beamformer

In addition to the A/Ds and DDCs, the 7153 includes essential resources of a complete beamforming subsystem. First, each DDC channel provides user-programmable I & Q phase and gain adjustments to apply beamforming weights. Then, a summation block adds the four DDC output channels.

An additional programmable-gain stage compensates for summation bit growth. A power meter and threshold detect block is provided for the sum output. The sum output is then delivered to the Channel 1 FIFO for delivery through the PCI-X bus.

For larger systems, multiple 7153's can be chained together using a built-in Xilinx Aurora engine. It accepts an x4 gigabit sum input stream from a previous board and propagates an x4 sum output stream to the next board through the P15 XMC connector.

Output Multiplexers and FIFOs

Four output MUXs can be independently switched to deliver either A/D or DDC data into each of the four output FIFOs. This allows users to view either the wideband A/D or the narrowband DDC data, depending on the application.

Each of the output FIFOs operates at its own input and output rate to support different DDC decimation settings between the channels and to enable efficient block transfers to the PCI-X bus.

Clocking and Synchronization

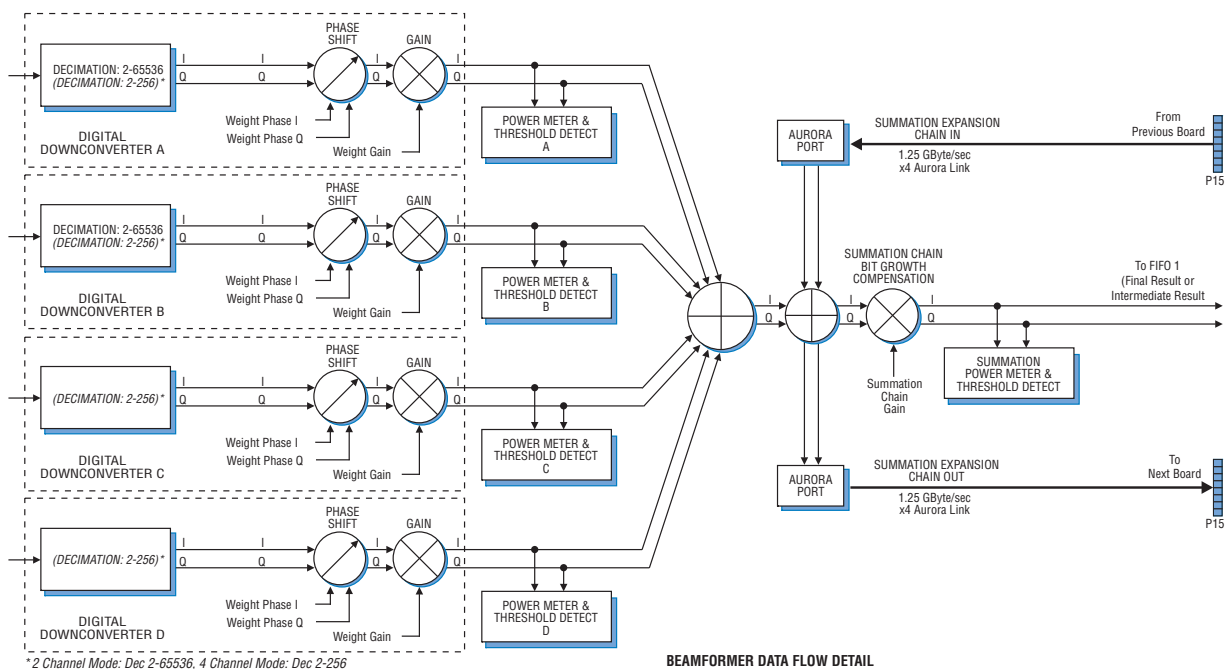
The Model 7153 architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven from the internal crystal oscillator, a front panel reference or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules. Up to three slave 7153's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. More modules may be synchronized with an external clock and sync generator.

PCI-X Interface

The Model 7153 includes an industry-standard PCI-X interface. The interface includes four separate DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33, 66 and 100 MHz are supported.



Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillator, external reference or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS, input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Digital Downconverter

Type: IP core for Xilinx Virtex-5

Qty of DDC Channels: 2 or 4

Center Frequency Tuning: 4 tuning words, one for each DDC channel

Center Frequency Tuning Range: DC to f_s with 32 bit resolution

NCO SFDR: -120 dBFS

Channel Phase Offset Adjustment: 32-bit resolution

Channel Gain Adjustment: 32-bit resolution

Input Selection for DDC Banks: Any channel can select any of the four A/Ds

Decimation Range (N):

2-Channel Mode: 2 to 65536

4-Channel Mode: 2 to 256

FIR Filter: Default passband $0.8 \cdot f_s / N$ with 0.2 dB passband ripple and 100 dB adjacent channel rejection

FIR Filter Coefficients: 18 bits, user-programmable (default values provided)

Qty FIR Filter Taps: $28 \cdot N / 8$

Output Format: 24 bits I + 24 bits Q

Output Spectrum Modes: Normal or frequency-reversed

Output Spectrum Offset: No offset or offset by one-half the output bandwidth

Beamformer

Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain

Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol

Phase Shift Coefficients: I & Q with 16-bit resolution

Gain Coefficients: 16-bit resolution

Channel Summation: 24-bit

Multiboard Summation Expansion: 32-bit

Output Multiplexer and FIFO

Qty Output FIFOs: Four

FIFO Source Selection: Independent multiplexer selects DDC output or A/D

PCI Interface

Type: IP core in Xilinx FPGA

PCI-X Bus: 64 bits, 100 MHz and 64 or 32 bits at 33 or 66 MHz

DMA: 4-channel demand mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7153	4-Channel DDC with four 200 MHz, 16-bit A/Ds and Beamformer - PMC/XMC

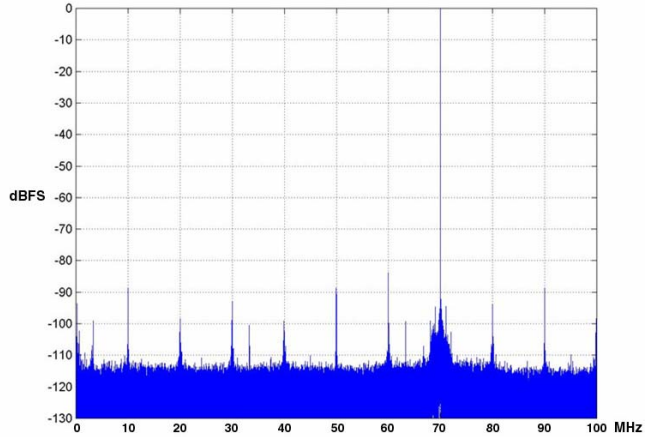
Options:

-730	Two-slot heat sink
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Contact Pentek for available options.

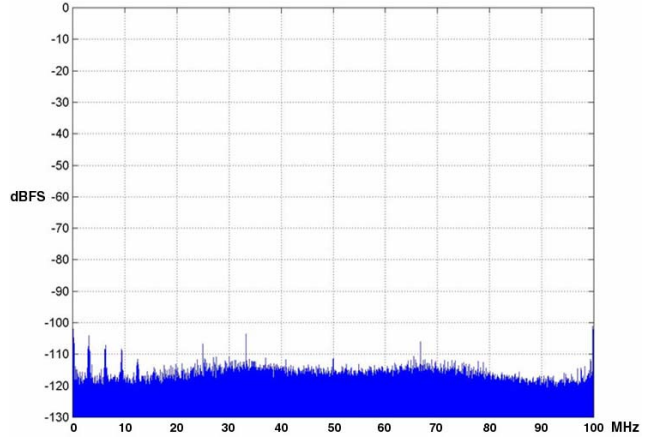
A/D Performance

Spurious-Free Dynamic Range



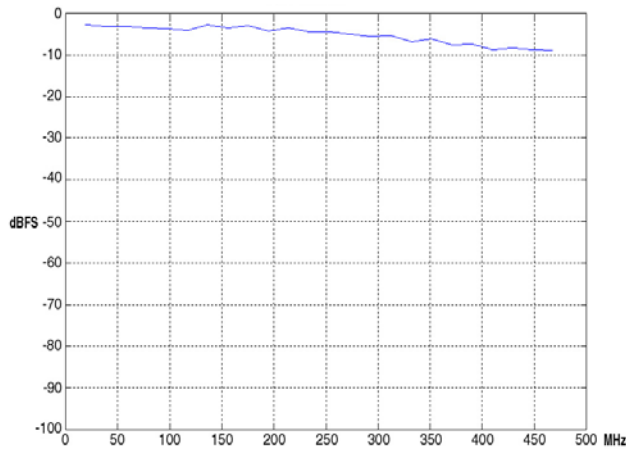
$f_{in} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Internal Clock}$

Spurious Pickup



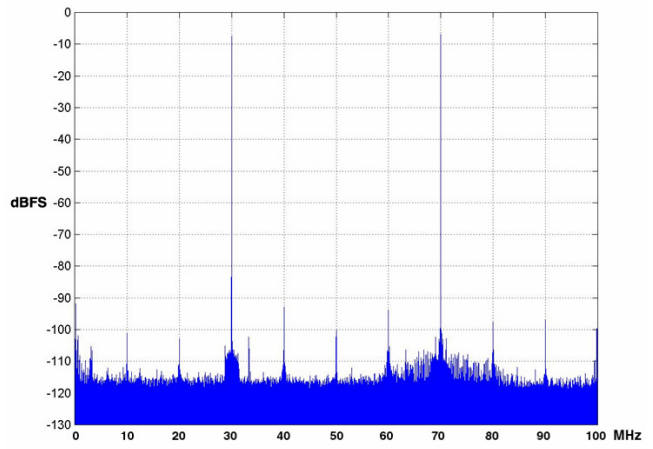
$f_s = 200 \text{ MHz}, \text{Internal Clock}$

Input Frequency Response



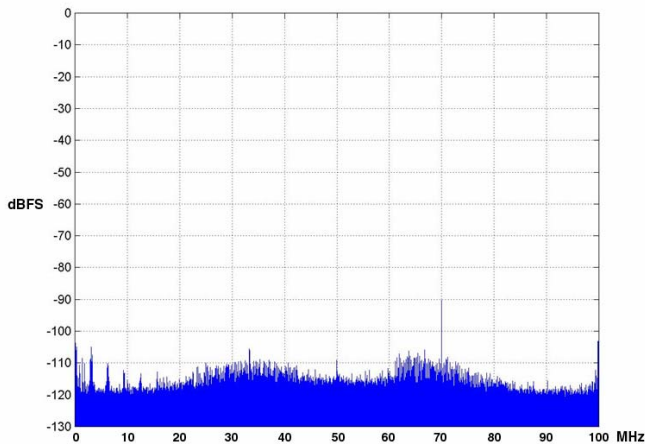
$f_s = 200 \text{ MHz}, \text{Int. Clock}$

Two-Tone SFDR



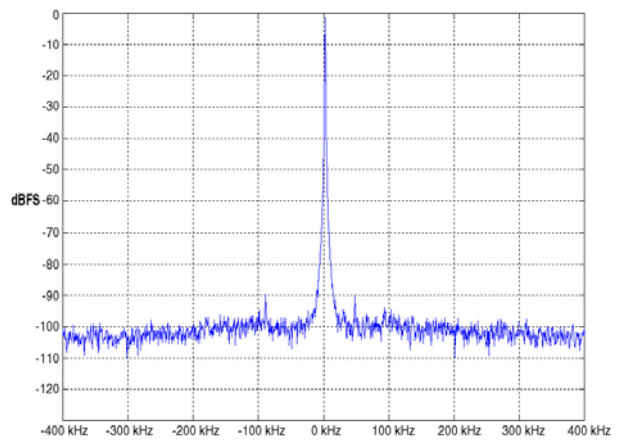
$f_{in1} = 30 \text{ MHz}, f_{in2} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Int. Clock}$

Adjacent Channel Crosstalk



$f_{in} = 70 \text{ MHz}, A_{in} = 0 \text{ dBFS}, f_s = 200 \text{ MHz}, \text{Int. Clock}$

Phase Noise at 70 MHz



$f_s = 200 \text{ MHz}, \text{Int. Clock}$