New!

Model 6823

4-Channel 500 MHz, 8-bit A/D with Virtex-4 FPGAs - VME

Preliminary Information

ReadyFlow Board Support Libraries

GateFlow

Features

- Four 500 MHz, 8-bit Atmel AT84AD004 A/D converters
- Wideband transformer-coupled inputs
- Ideal for IF sampling at frequencies up to 800 MHz
- Four Xilinx Virtex-4 XC4VSX55 FPGAs
- Control and status via VMEbus
- Front panel gate and trigger
- Multiboard synchronization

Ordering Information

Model	Description
6823	4-Channel 500 MHz, 8-bit A/D with Virtex-4 FPGAs - VME

General Information

The Model 6823 is a high-frequency four channel A/D converter in a 6U VME-bus form factor. It accepts four front panel analog inputs and delivers digital output samples over a FPDP (front panel data port) connector utilizing FPDP or FPDP II standards.

The Model 6823 is ideal as a high-speed data acquisition front end for real-time recording, digital receivers and digital signal processing systems.

Input Stage and A/D Converter

A front panel female SMA connector accepts an analog RF input at a full scale level of -2 dBm into the primary of a RF transformer which presents a 50 ohm input impedance. The transformer provides a flat frequency response from 300 kHz to 800 MHz. The transformer offers a low-distortion path to the differential inputs of the Atmel AT84AD004 A/D converters and minimizes system noise and ground loops.

Clocking, Gating and Triggering

The A/D converter sample clock is derived from an external sinusoidal source at a maximum frequency of 500 MHz.

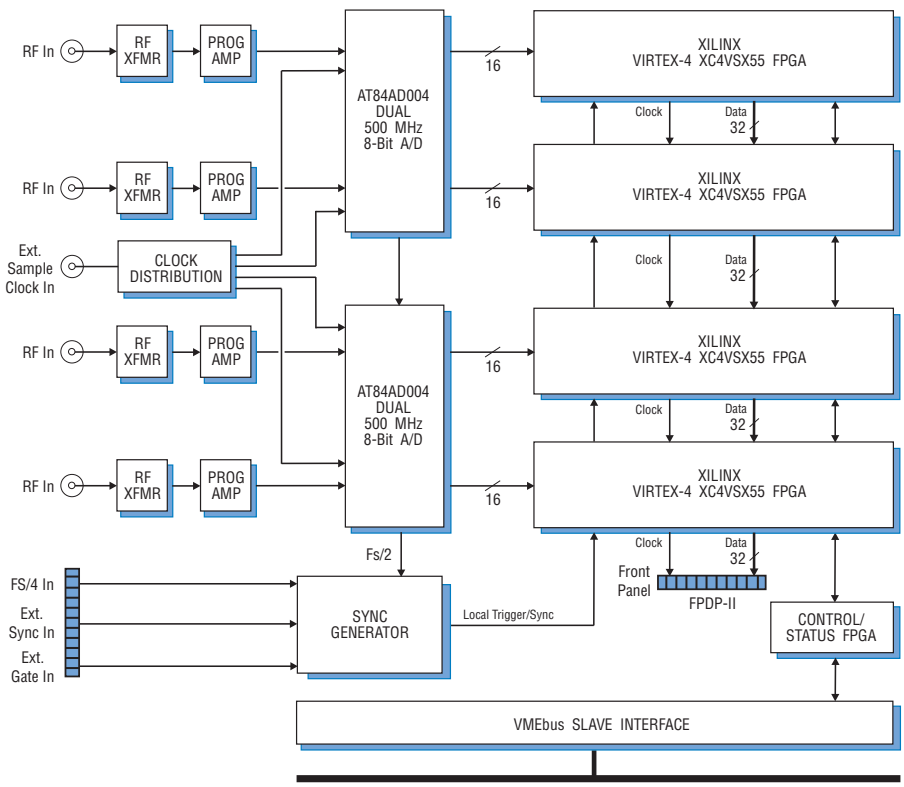
This clock is accepted through a front panel SMA connector terminated in 50 ohms.

An external LVDS timing bus supports synchronous data acquisition across multiple boards. This is ideal for applications such as multichannel radar systems where several A/D converters must capture transient records at precisely the same sample time.

Virtex-4 FPGAs

The 6823 utilizes four Xilinx Virtex-4 XC4VSX55 FPGAs. As the largest FPGA in the SX family, the XC4VSX55 is rich in processing resources. Each FPGA contains 512 XtremeDSP Slices, 5,760 kbits of block RAM and 55,296 logic cells. The XC2V4SX55s easily accept any of Pentek's GateFlow IP Cores including: Core 421 Wideband 160 MHz DDC, Core 422 Wideband 296 MHz DDC, Core 430 256-Channel Narrowband DDC Bank and Core 440 Pulse Compression Core. In addition, an optional Model 4953-823 GateFlow Design Kit, assists developers in creating custom IP for the 6823's FPGAs.

Each FPGA accepts parallel digital signals at the sampling frequency from the A/D converter. Each FPGA is connected to the next via a 36-bit parallel bus. The last FPGA in the chain presents the 36-bit data at the front panel FPDP connector. This architecture supports channelized applications such as communication systems and data summation applications such as beamforming.



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