Model 6256

Dual/Quad 105 MHz A/D w/Virtex-II Pro FPGA - VIM-2

ReadyFlow Board Support Libraries

GateFlow

Features

- Complete software radio front end
- Up to four 105 MHz 14-bit A/D Converters
- Two user-configurable Virtex-II Pro FPGAs
- On-board auxiliary SDRAM and FLASH memory
- External clock input
- LVDS clock/sync bus for multi-module synchronization
- GateFlow FPGA Design Kit and IP Cores

Ordering Information

Model Description

6256	2-Channel A/D with Virtex-II Pro FPGA - VIM-2

Options

-009	4-Channel Version (Second-Slot Dual A/D Mezzanine)
-020	XC2VP20 FPGAs
-050	XC2VP50 FPGAs

General Information

The Model 6256 is a complete two or four channel data acquisition and signal processing subsystem implemented as a VIM-2 module. Up to two 6256 modules can be attached to any of the Pentek VIM baseboards for a total of eight channels.

The 6256 is ideal for digitizing signal bandwidths up to 45 MHz with subsequent real-time digital signal processing and data buffering of those signals using two on-board Xilinx Virtex-II Pro FPGAs.

A/D Converters

The front end accepts two full scale analog HF or IF inputs at +4 dBm full scale into 50 ohms on front panel SMA connectors. Each input is transformer coupled, and digitized by a 14-bit 105 MHz A / D converter (Analog Devices AD6645).

The A / D converters deliver parallel digital output into a Virtex-II Pro FPGA for further processing. An optional second-slot mezzanine provides two additional A / D converters. These deliver output to a second Virtex-II Pro for a 4-channel system.

The A / D clock can be driven from an internal crystal oscillator or from an external sample clock supplied through a front panel SMA connector. A front panel LVDS clock and sync bus supports synchronization across multiple modules. For large, multi-channel systems, up to 80 modules can be synchronized using the Model 9190 Clock and Sync Generator.

Virtex-II Pro FPGAs

The Model 6256 is equipped with a pair of FPGA devices from the Xilinx Virtex-II Pro family. Models XC2VP20 or XC2VP50 are selectable by option number. Contact factory for alternate sizes.

Each Xilinx Virtex-II Pro FPGA includes factory installed functions for data formatting, channel selection, timing, triggering and gating. In addition to ample on-board SRAM memory and configurable logic, each FPGA features two PowerPC processor cores for implementing internal control or analysis functions.

These resources are available to customers for implementing extremely powerful signal processing algorithms for signal intelligence, radar, communications, process control, and test instrumentation.

Memory Resources

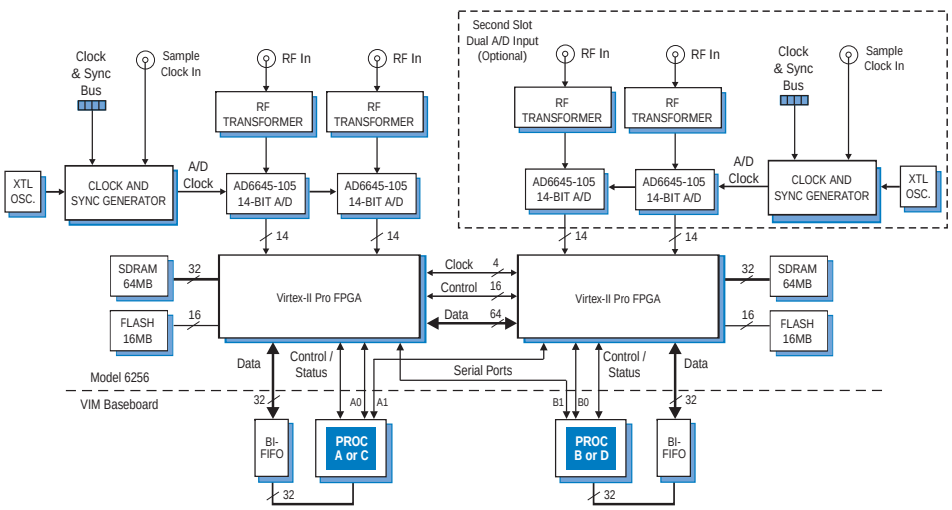
Each FPGA is equipped with a 64 MB SDRAM connected with separate address and data buses so it can be used independently. These SDRAMs are useful for storing data without consuming internal FPGA logic cells. In addition, 16 MB of FLASH memory is attached to each FPGA (32 MB total).

VIM Processor Interface

The FPGA outputs are connected through the VIM mezzanine interface to the 32-bit synchronous FIFO on the VIM processor board where it is buffered for efficient block transfers into the baseboard processor.

FPGA Programming

Pentek's optional GateFlow Design Kit allows the FPGAs to be configured by the user for implementation of custom preprocessing functions such as FFTs, FIR filters, compression and decompression algorithms, software radio blocks, decryption, telemetry functions, decoders and encoders, and convolution.



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