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Features

- Mezzanine card for Pentek 429x processor family
- Dual 14-bit, 105 MHz A/Ds
- Dual GateFlow Core 421, high-performance wideband digital downconverter core, factory-installed
- Improved dynamic range
- Four sets of 18-bit user-programmable FIR filter coefficients
- Optional GC1012B digital downconverters offer decimation factors up to 4096

Ordering Information

6236 Model 6236 14-bit A/D - VIM-2

Options:

- 300-421 Wideband DDC Core
- 212 With two GC1012B DDC ASICs

General Information

Model 6236-421 Dual Wideband GateFlow Digital Receiver includes two complete acquisition and receiver channels in a VIM-2 mezzanine module compatible with all VIM-compatible platforms, including the Pentek 429x series processor boards.

The 6236 features two AD6645 105 MHz 14-bit A/D converters and optional GC1012B wideband digital downconverters. Because the GC1012B DDCs accept only 12-bit digital inputs, the resolution of the additional two A/D bits is lost.

To address this issue, Pentek developed the GateFlow IP Core 421 High-Performance Wideband DDC similar in functionality to the Texas Instruments' GC1012B, but with enhanced speed, performance and programmability. It accepts a full 16 bits of input data in either real or complex format, taking full advantage of the 14-bit A/D converters.

In standard 6236 units, the Virtex-II FPGA contains factory-programmed code to implement control, initialization, mode selection and data formatting functions. Since much of the FPGA remains available for custom signal processing algorithms, Pentek offers the 4236-421 as a factory installation of two complete channels of the GateFlow IP Core 421. The XC2V3000 is required to accommodate this configuration.

Architecture

The block diagram below shows the AD6645 A/D converter driving an optional GC1012B and also bypassing the GC1012B for a direct connection to the FPGA. A programmable switch allows the FPGA input to be either the real A/D out-

put or the complex output from the GC1012B.

This arrangement allows customers to purchase the product without the GC1012B chips installed, or to cascade the GC1012B and the Core 421 receiver to achieve additional decimation up to a factor of 4096, instead of 64 for either receiver alone.

Core 421 Receiver

Like the GC1012B, the Core 421 DDC translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter then removes any out of band frequency components. An output decimator and formatter delivers output data in several different formats in either real or complex representation.

An input gain block allows both the I and Q data streams to be multiplied by a 16-bit gain term. The NCO provides over 118 dB spurious-free dynamic range (SFDR). The mixer utilizes four 18x18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. The FIR filter is capable of storing and utilizing up to four independent coefficient sets of 18-bit coefficients for each decimation value. Two default coefficient sets are preprogrammed for 80% and 90% passband filters with characteristics shown below.

Default Filter	Usable Bandwidth	Passband Ripple	Stopband Rejection
80%	0.8 Fs	< 0.08 dB	> 100 dB
90%	0.9 Fs	< 0.50 dB	> 75 dB

Fs = Complex Output Sample Rate

