# Model 6232

# 32-Ch. Narrowband Receiver with FPGA, FPDP Inputs - VIM-4

GateFlow ReadyFlow Board Support Libraries

## Features

- Four 16-bit digital inputs on two FPDP connectors
- Dual Field Programmable Gate Arrays (FPGAs)
- Front panel FPGA I/O
- All downconverters can select any of the four inputs
- 40 MHz input clock rate ($f_s$)
- 2 kHz to 1 MHz output bandwidths for $f_s$ = 40 MHz
- Front panel clock/sync bus for board synchronization

## Ordering Information

| Model | Description |
|---|---|
| 6232 | 32-Channel Narrowband Receiver with FPGA, FPDP inputs - VIM-4 |
| **Option:** | |
| -600 | XCV600E FPGAs |

## General Information

Model 6232 is a general-purpose 32-channel narrowband digital receiver VIM-4 module. It attaches to VIM-compatible processor boards and connects directly to all four processors.

## Front End

The Model 6232 accepts four 16-bit digital inputs on two front panel FPDP connectors supporting data rates up to 40 MHz. Data from each 16-bit input flows into a FIFO to allow synchronization, and is in turn transferred to the digital receiver section. Data from any of the four inputs can be directed to any of the 32 receiver channels or directly to the FPGAs.

Each FPDP connector is clocked individually. Clock information is sent to a controller for data clocking and sync.

## Digital Downconverters

The 6232 includes eight Graychip GC4016 quad narrowband digital downconverter chips. The maximum input sampling rate for the GC4016 is 80 MHz. Each device includes four independently tuned channels capable of center frequency tuning from DC to 20 MHz, and with output bandwidths ranging from 2 kHz to 1 MHz (for 40 MHz sample clock).

Each GC4016 accepts up to three 16-bit or four 14-bit parallel inputs from the input FIFOs. Internal crossbar switches allow all 32 downconverter channels on the board to select any of the four inputs for flexible switching.

## Synchronization

The front panel clock and sync bus allow one 6232 to act as a master, driving the sample clock out to a front panel cable bus using LVDS differential signaling. Multiple slaves can then be clocked synchronously with the master. Additional sync lines on the bus allow synchronization of the local oscillator phase, frequency switching, decimating filter phase, and FIFO data collection on multiple 6232's.

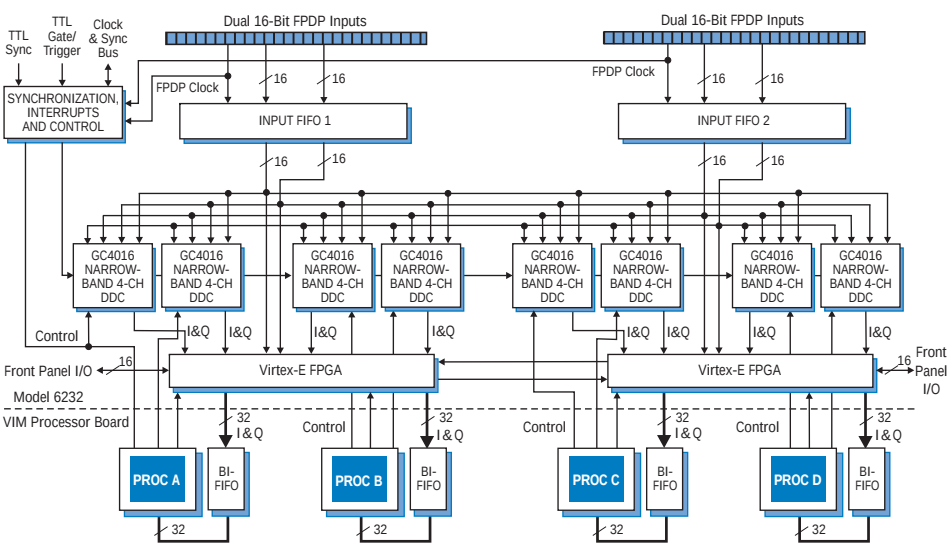
## FPGAs

The downconverter outputs are delivered to two Xilinx Virtex-E Series XCV300E FPGAs (Field Programmable Gate Arrays) which perform various modes of data packing, formatting and channel selection. Xilinx Model XCV600E FPGAs are optionally available for more extensive applications.

Optionally available GateFlow Design Kits allow the FPGAs to be configured by the user for implementation of custom preprocessing functions such as convolution, framing, pattern recognition and decompression.

## VIM Processor Interface

The FPGA outputs are connected directly through the VIM mezzanine interface to the 32-bit synchronous FIFO on the VIM baseboard where it is buffered for efficient block transfers into the processor. The processor can control the programmable registers on its associated GC4016's as well as control and initiate sync bus functions.





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