Model 6231

16-Ch. Narrowband Receiver with A/D and FPGA - VIM-2

GateFlow ReadyFlow Board Support Libraries

Features

- Two 65 or 80 MHz, 14-bit A/D converters
- Optional front panel FPGA I/O connector
- All downconverters can select any of the two inputs
- 90 MHz input bandwidth
- 3.2 kHz to 1.6 MHz output bandwidths for f_s = 64 MHz
- Front panel clock and sync bus synchronize multiple boards
- See Model 7131 for PMC version

General Information

The Model 6231 is a general-purpose 16-channel narrowband digital receiver VIM-2 module. It attaches directly to VIM-compatible processor boards and connects directly to two processors.

Front End

Model 6231 accepts two analog RF inputs at +4 dBm full scale into 50 ohms on front panel SMA connectors. Amplifier bandwidth of 90 MHz supports direct IF undersampling. Each input is amplified and, optionally, lowpass filtered to remove out-of-band signals and prevent aliasing. The filters may be bypassed for undersampling applications.

Optionally available, transformer-coupled inputs reduce distortion for input signals above 10 MHz and are recommended for IF undersampling applications.

Each of the two inputs is then digitized by a 14-bit A/D converter which is capable of operating at sample rates up to 65 MHz (Analog Devices AD6644) or, optionally, 80 MHz (AD6645). The A/D converter clock can be driven from an internal 64 MHz or 80 MHz crystal oscillator, or from an external sample clock supplied through a front panel SMA connector.

Digital Downconverters

The 6231 includes four Graychip GC4016 quad narrowband downconverter chips. The maximum input sampling rate for the GC4016 is 80 MHz. Each device includes four independently tuned receiver channels capable of center frequency tuning from DC to 32 MHz, and with output bandwidths ranging from 3.2 kHz to 1.6 MHz (for 64 MHz sample clock).

Each GC4016 accepts four 14-bit parallel inputs from the two A/D converters. Internal crossbar switches allow all 16 channels on the board to select either of the A/D inputs for flexible switching.

Synchronization

The front panel clock and sync bus allow one 6231 to act as a master, driving the sample clock out to a front panel cable bus using LVDS differential signaling. Multiple slaves can then be clocked synchronously with the master. Additional sync lines allow synchronization of the local oscillator phase, frequency switching, decimating filter phase, and FIFO data collection on multiple 6231's.

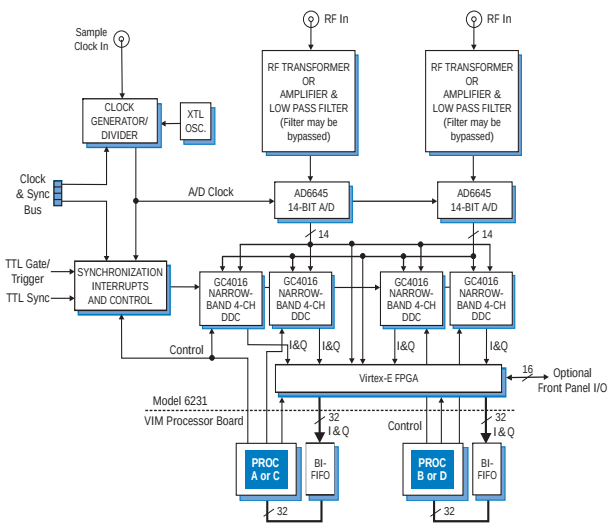
FPGA

The 16 downconverter outputs are delivered to a Xilinx Virtex-E Series XCV300E FPGA (Field Programmable Gate Array) which performs various modes of data packing, formatting and channel selection. The A/D outputs are also connected directly to the FPGA so that wideband A/D data can be delivered directly to the processor board, bypassing the downconverters. Xilinx Model XCV600E FPGA is optionally available for more extensive applications.

Optionally available GateFlow Design Kits allow the FPGAs to be configured by the user for implementation of custom preprocessing functions such as convolution, framing, pattern recognition and decompression.

VIM Processor Interface

The FPGA output is connected directly through the VIM mezzanine interface to the 32-bit synchronous FIFO on the VIM processor board where it is buffered for efficient block transfers into the processor. The processor can control the programmable registers on its associated GC4016's as well as control and initiate sync bus functions.



Ordering Information

Model	Description
6231	16-Channel Narrowband Receiver with A/D and FPGA - VIM-2
Options:	
-080	80 MHz A/Ds and internal oscillator
-102	Front Panel FPGA I/O (requires additional VMEbus slot)
-105	Transformer-coupled input
-600	XCV600E FPGA

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