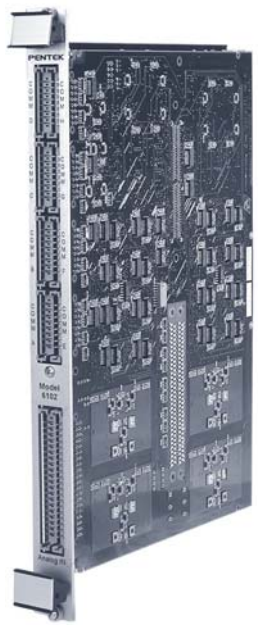
Model 6102

8-Channel 16-bit 250 kHz A/D & D/A - VME



General Information

Model 6102 is a high-performance 8-channel A/D & D/A converter for VMEbus data acquisition, control, and DSP applications. Model 6102 offers differential inputs, 16-bit resolution and sampling frequencies to 250 kHz.

Digitized data is stored in independent 1 ksample FIFOs, while 16-ksample FIFO depth is optionally available.

As a full depth MIX module, the Model 6102 may be attached directly to a DSP processor using the Intel MIX mezzanine bus. This 32-bit bus allows up to three MIX modules to be attached to a MIX baseboard, such as the Pentek 428x series of DSP MIX Baseboards, or the Pentek 4200 series of MIX to VME Baseboards.

Interfaces

Digital I/O data can be delivered to the VMEbus, the MIX bus, or to front panel C40-compatible comm ports. Each of the eight comm ports supports a pair of converters, with four comm ports for A/D's and four for D/A's.

The VMEbus and MIX bus have full memory mapped slave access to all data FIFOs, interrupt controls, sample rate generators, and control registers.

All input and output FIFOs can be configured under software control to interrupt the MIX bus or VMEbus on full, half-full and empty conditions.

Sampling Rate Control

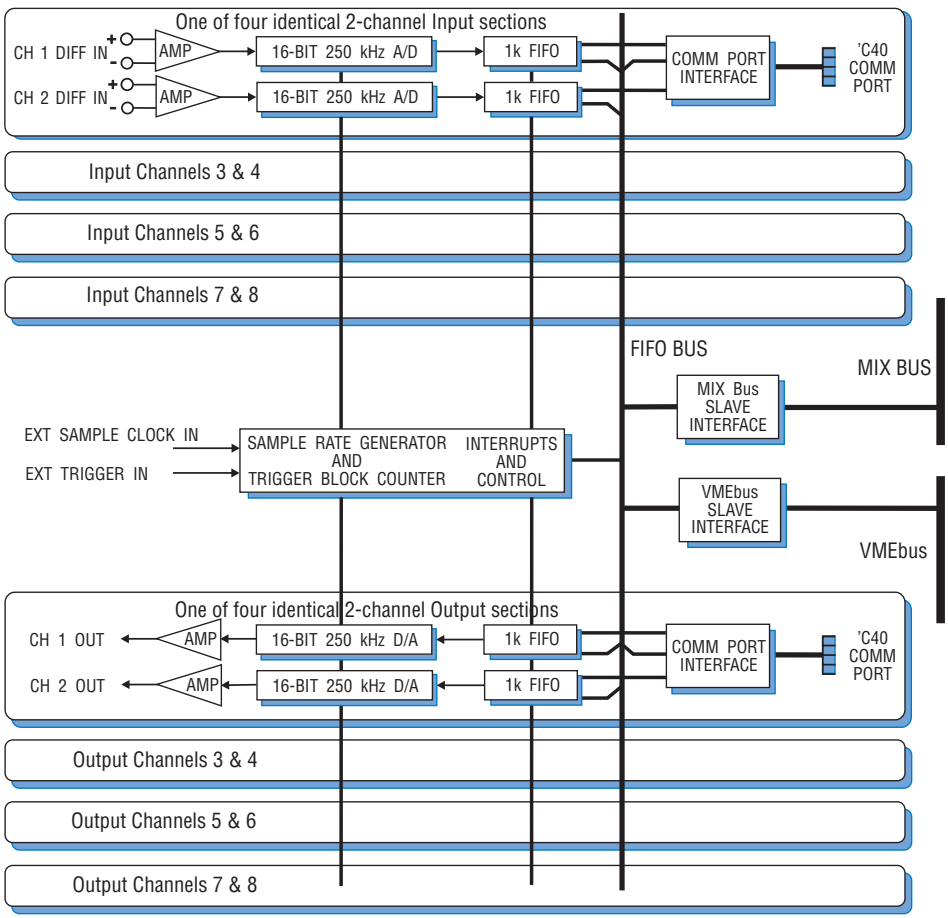
The sampling clock can be supplied from one of four internal sample rate generators, or an external TTL sampling clock. Sampling rates up to 250 kHz for all converters are supported.

Applications

The Model 6102 is ideal for real-time process control applications where latency and loop delay must be minimized. As each sample is converted, it is immediately available to the interface because of the ➤

Features

- 8 analog I/O channels
- 16-bit resolution with simultaneous sampling
- Differential inputs
- VME, MIX and C40 comm port interfaces
- Internal or external sampling clocks to 250 kHz
- FIFO buffering for each A/D and D/A channel



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➤ near-zero fall through time for the FIFOs. Thus, each channel can be directly addressed by the processor, one sample at a time.

Specifications

Input Channels
- **Number:** eight, any channel may be enabled or disabled
- **Input:** differential, ±5.0 V full scale, 100 kohm input impedance; common mode rejection >60 dB at 60 Hz.

A/D Converters
- **Type:** ADS7811
- **Sampling rate:** DC to 250 kHz
- **Resolution:** 16 bits
- **THD:** <–87 dB below FS
- **IM distortion:** <–85 dB below FS
- **SINAD:** >80 dB

(specifications apply with 10 kHz input frequency)

Input FIFO: 1 ksample per A/D channel, optionally expandable to 16 ksample

Output Channels
- **Number:** eight, any channel may be enabled or disabled
- **Output:** single-ended, ±5.0 V full scale, 50 ohm output impedance

D/A Converters
- **Type:** AD569
- **Sampling rate:** DC to 250 kHz
- **Resolution:** 16 bits
- **Glitch energy:** 300 nV-sec, typical

D/A Converters (Option -014)
- **Type:** LTC1597
- **Sampling rate:** DC to 250 kHz
- **Resolution:** 16 bits
- **Glitch energy:** 2 nV-sec, typical

Output FIFO: 1 ksample per D/A channel, optionally expandable to 16 ksample

Sampling Clocks
- **Frequency dividers:** four, each selectable for any A/D or D/A pair; each divides internal or external reference by N, where N = 1 to 65536
- **Internal reference:** 20 MHz (±100 ppm)
- **External reference:** 20 MHz max. optically-isolated TTL-compatible front panel input

Trigger/Gate Control
- **Input:** optically-isolated TTL-compatible front panel input, or VMEbus control bit
- **Trigger mode:** positive or negative edge starts conversion
- **Gate mode:** logic '0' or '1' enables conversion
- **Sample counter:** generates VMEbus interrupt N samples after trigger, where N = 2 to 256

Comm Port Interface
- **Number:** eight C40-compatible comm ports, one per pair of A/D's and one per pair of D/A's
- **Data and control lines:** eight data plus four control lines each
- **Data format:** data is always transferred as four eight-bit bytes forming a 32-bit C40 long word
- **Combined Port Mode**
  - **Transfers:** one comm port handles data for up to eight A/D or D/A channels in non-packed mode; one 16-bit sample is left-justified in 32-bit long word; three LSB's indicate channel ID
- **Independent Port Mode**
  - **Transfers:** each comm port handles data for one or two A/D or D/A channels in packed or non-packed mode
  - **Non-packed:** one 16-bit sample left-justified in 32-bit long word; only one channel enabled per pair
  - **Packed:** two 16-bit samples in 32-bit long word

VMEbus Interface
- **Type:** slave A32 D32 I(1-7)
- **Transfers:** BLT (block level transfers), 16 k range per FIFO
- **Control registers:** sample clock divisors, trigger/gate control, interrupt mask, channel enables, clock source, comm port modes, FIFO resets, A24/A32 base address, interrupt vector register
- **Status registers:** interrupt status, FIFO flags
- **Memory map:** all FIFOs, control and status registers are mapped into A16 space; FIFOs are also mapped into A24/A32 space
- **Maskable interrupts:** FIFO status (full, half-full or not-empty conditions) and sample counter

MIX interface: 32-bit slave; memory-mapped FIFO, status/control, interrupt mask registers and programmable sample rate divider; maskable FIFO interrupts on empty, half full and full

Power: 3.0 A at +5 V; 0.5 A at ±12 V

Size: standard 6U VMEbus board, single slot; board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 0.8 in. wide

Ordering Information

Model	Description
6102	8-Channel 16-bit 250 kHz A/D and D/A - VME
Options:	
-002	16 ksample FIFO, D/A section only
-003	16 ksample FIFO, A/D section only
-014	Low glitch energy D/A, low latency