New!

Models 57611 and 58611

Quad or Octal Serial FPDP Interface with Virtex-6 FPGA - 6U OpenVPX

Model 58611

General Information

Models 57611 and 58611 are members of the Cobalt® family of high performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71611 XMC modules mounted on a VPX carrier board.

Model 57611 is a 6U board with one Model 71611 module while the Model 58611 is a 6U board with two XMC modules rather than one.

These models are fully compatible with the VITA 17.1 Serial FPDP specification. Their built-in data transfer features make them complete turnkey solutions. For users who require application-specific functions, they serve as flexible platforms for developing and deploying custom FPGA processing IP.

The Cobalt Architecture

The Pentek Cobalt Architecture features one or two Virtex-6 FPGAs. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

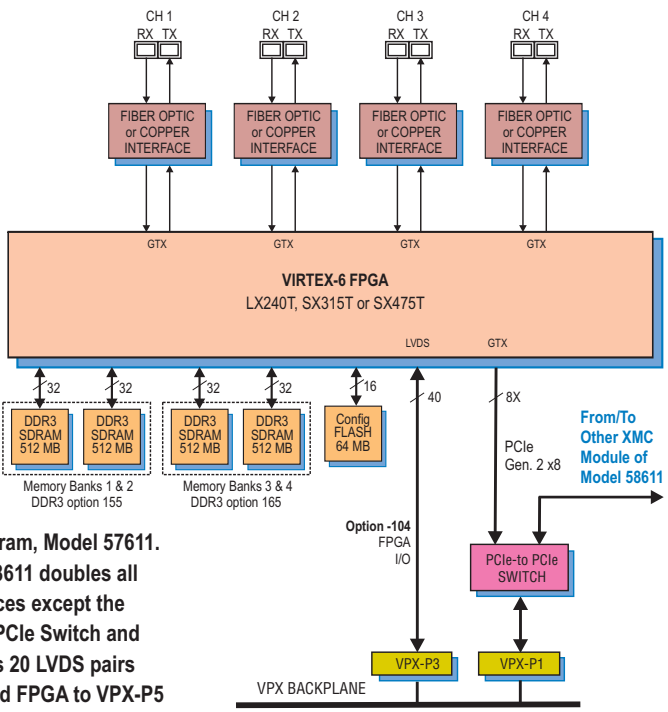
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57611; P3 and P5, Model 58611. ➤

Cobalt GateFlow ReadyFlow Board Support Package

Features

- Four or eight channels of serial FPDP interface
- Fully compliant with VITA 17.1specification
- Fiber optic or copper serial interfaces
- One or two Virtex-6 FPGAs
- Up to 2 or 4 GB of DDR3 SDRAM
- PCI Express interface up to x8
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57611. Model 58611 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

PENTEK

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Models 57611 and 58611

Quad or Octal Serial FPDP Interface with Virtex-6 FPGA - 6U OpenVPX

➤ Serial FPDP Interface

These models are fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the boards can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

Memory Resources

The architecture supports up to four or eight independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Serial FPDP Inputs/Outputs
- **Number of Connectors:** 4 or 8
- **Fiber Optic Connector Type:** LC
  - **Laser:** 850 nm (standard, other options available)
- **Copper Connector Type:** Micro Twinax
- **Fiber Optic or Copper Link Rates:** 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)
- **Fiber Optic or Copper Data Transfer Rates:** 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Arrays: Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T

Custom I/O
- **Option -104:** Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57611; P3 and P5, Model 58611

Memory
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI Express Interface
- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

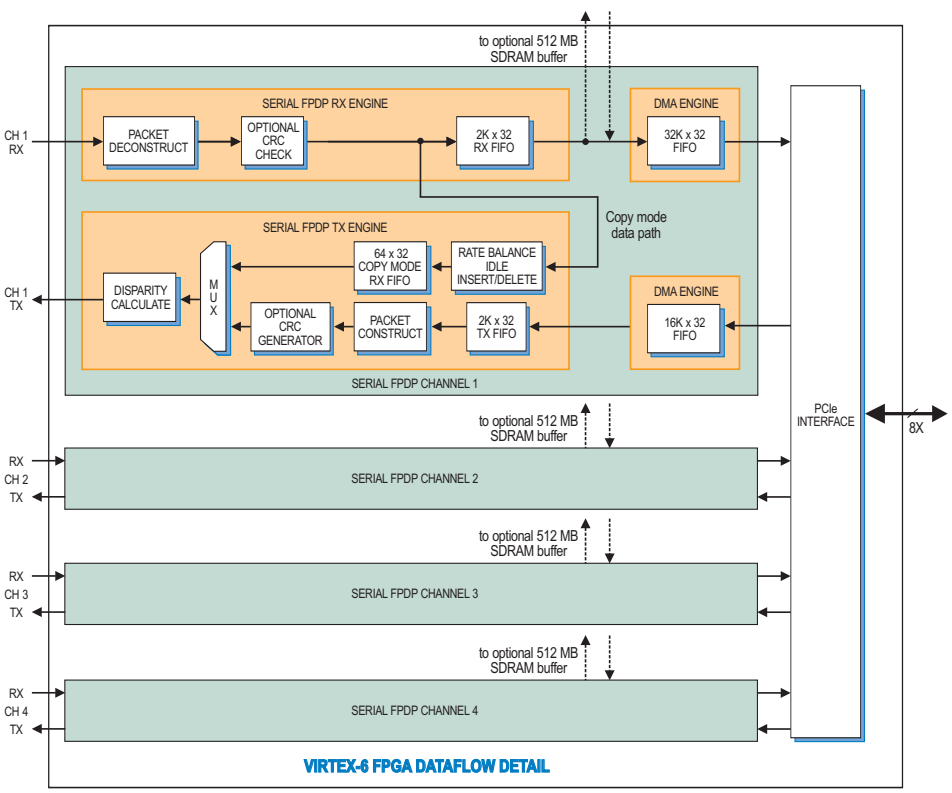
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm) ➤

Ordering Information

Model	Description
57611	Quad serial FPDP Interface with Virtex-6 FPGA - 6U VPX
58611	Octal serial FPDP Interface with two Virtex-6 FPGAs - 6U VPX
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-065	XC6VSX475T FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57611; P3 and P5 connectors, Model 58611
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-280	Copper serial interfaces
-281	Multi-mode optical serial interfaces

Contact Pentek for availability of rugged and conduction-cooled versions



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➤ Serial FPDP VITA 17.1 Compliance

These models comply fully with the VITA 17.1 specification as follows:

What Link Rate does the interface support?
■ 1.0625 Gbaud ■ 2.125 Gbaud ■ 2.5 Gbaud ■ 3.125 Gbaud ■ 4.25 Gbaud

What Serial FPDP function does the interface support?
__ Transmitter only __ Receiver only ■ Transmitter & Receiver

Does the Receiver support Flow Control (setting the STOP signal)?
__ Always active __Not supported ■ Optional (selectable)

Does the Transmitter support Flow Control (stopping data transmission on receipt of a STOP signal)?
__ Always active __ Not supported ■ Optional (selectable)

If the Transmitter supports Flow Control, after transmitting a STOP signal, how many 32-bit words can be received before a Receive FIFO overflow occurs?
■ Programmable

Does the interface support CRC?
__ Always active __ Not supported ■ Optional (selectable)

Does the Transmitter support Copy Master Mode (insertion of additional IDLE ordered sets)?
__ Always active __ Not supported ■ Optional (selectable)

Does the Receiver support Copy Mode (retransmission of data)?
■ Yes __ No

If Copy Mode is supported, what method is used for implementation (see VITA 17.1 Observation 6.1.4.4)?
__ Method 1 ■ Method 2

Does the Receiver support Copy/Loop Mode (retransmission of data and setting Flow Control)?
■ Yes __ No

What type of media is supported?
■ Short Wave Laser ■ Long Wave Laser ■ Copper

What type of media connectors are supported?
■ LC __ SC __ ST ■ Micro Twinax

Which fiber transmit data frames are supported in addition to Normal Data Fiber Frames (see VITA 17.1 Permission 7.3.3.1)?
■ Sync without Data Fiber Frames ■ Sync with Data Fiber Frames

Does the Serial FPDP Transmitter stop in response to the Serial FPDP Receiver sending NRDY True (see VITA 17.1 Observation 7.3.2.2)?
__ Always __ Never ■ Optional (selectable)

Are status bits kept up to date when there is no data to transmit by sending empty Serial FPDP Normal Data Fiber (see VITA 17.1 Rule 7.3.3.8, Recommendation 7.3.3.2 and Suggestion 7.3.3.1)?
■ Yes, empty frames transmitted __ No, status is not updated when no data is transmitted