



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 56660 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56660 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56660 to operate as a complete turnkey solution without the need to develop any FPGA IP.

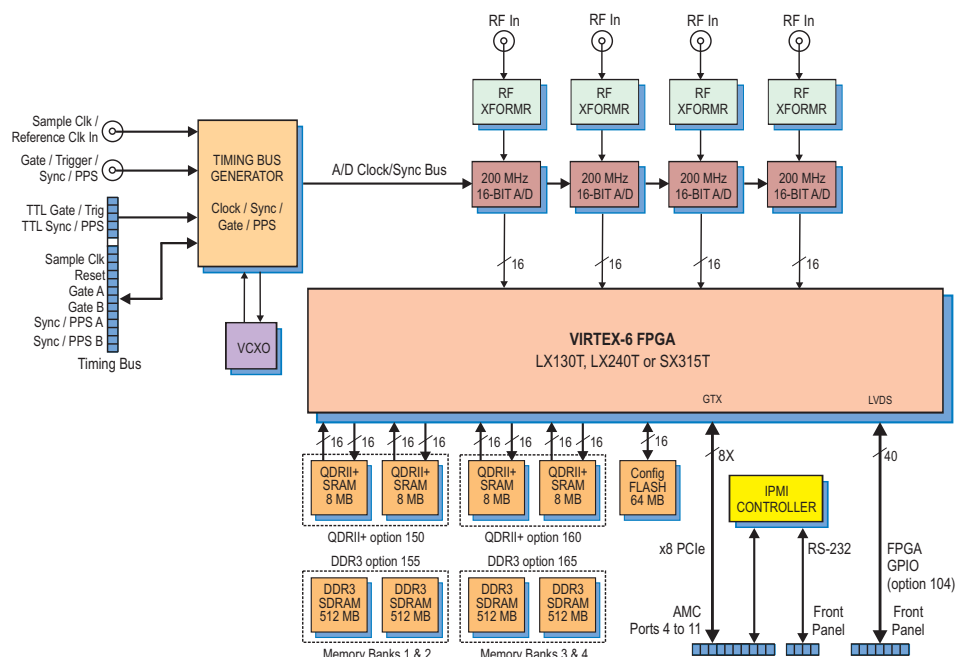
Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤



► A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the

LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

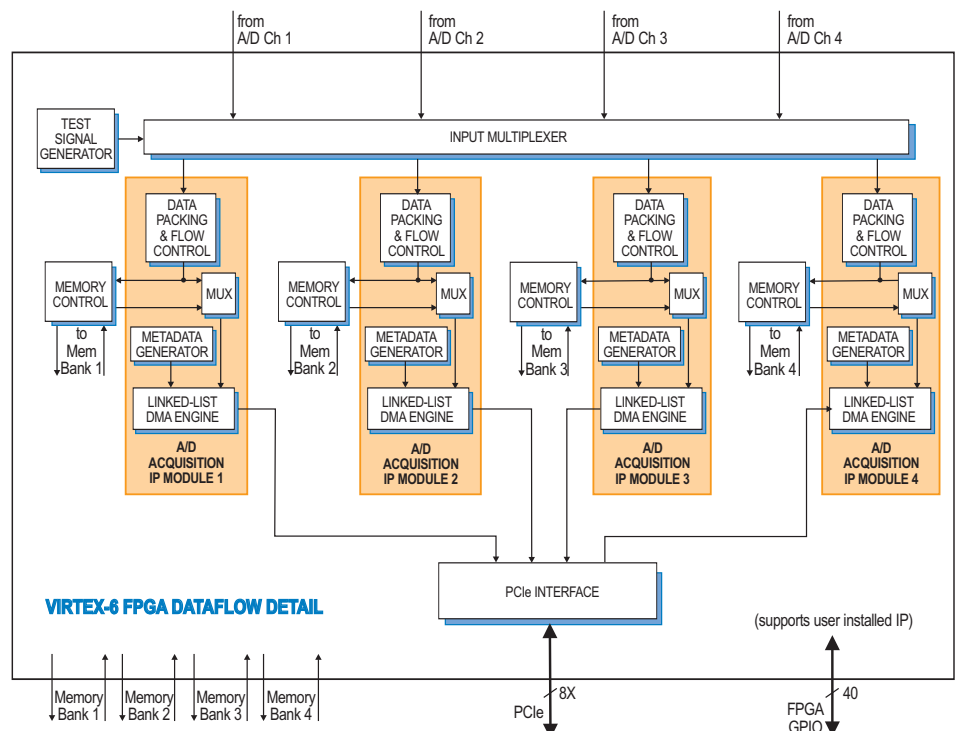
The Model 56660 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or μ TCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller). ►

A/D Acquisition IP Modules

The 56660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



► PCI Express Interface

The Model 56660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T

Optional: Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O

Option -104: Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

PCI Express Bus: Gen. 1: x4 or x8; Gen. 2: x4

AMC Interface

Type: AMC.1

Module Management: IPMI Version 2.0

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56660	4-Channel 200 MHz A/D with Virtex-6 FPGA - AMC

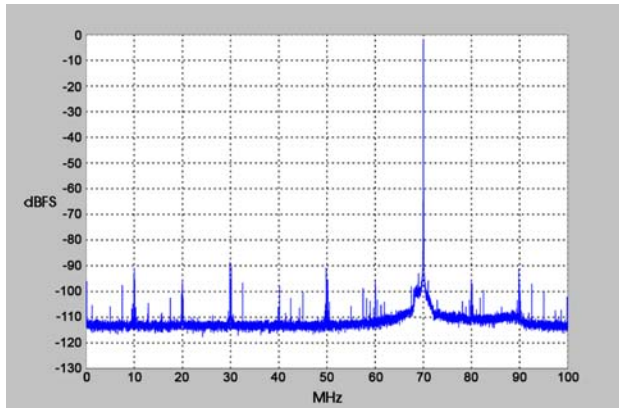
Options:

-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O through front panel connector
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

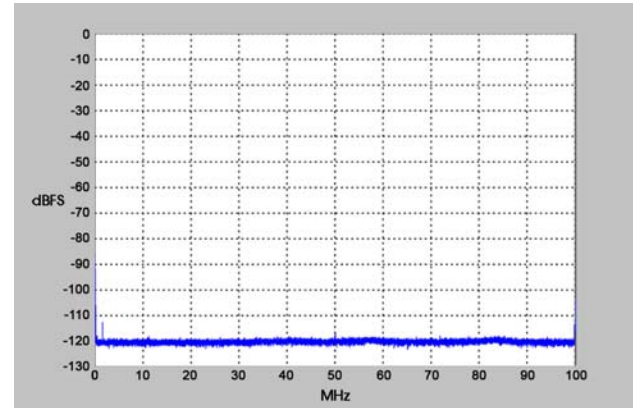
Contact Pentek for availability of rugged and conduction-cooled versions

A/D Performance

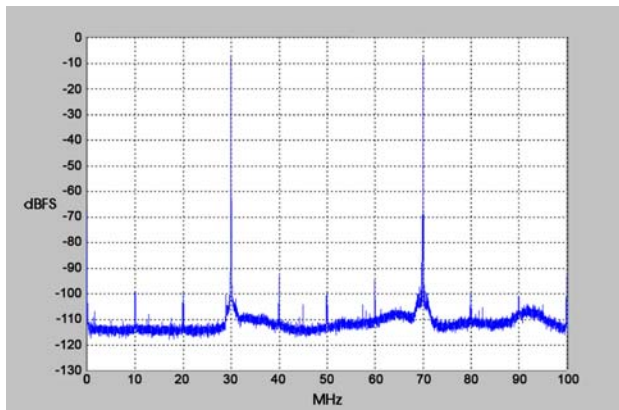
Spurious Free Dynamic Range


 $f_{in} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Internal Clock}$

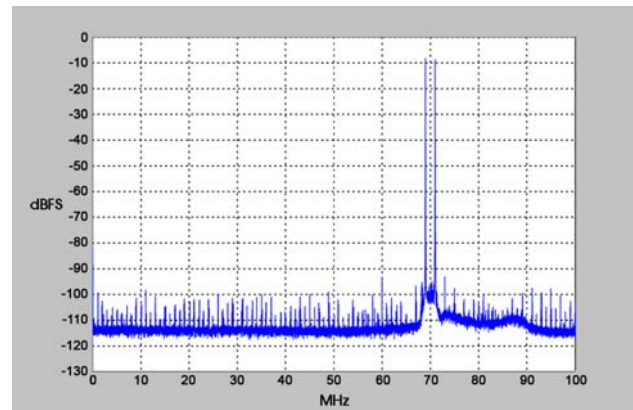
Spurious Pick-up


 $f_s = 200 \text{ MHz}, \text{Internal Clock}$

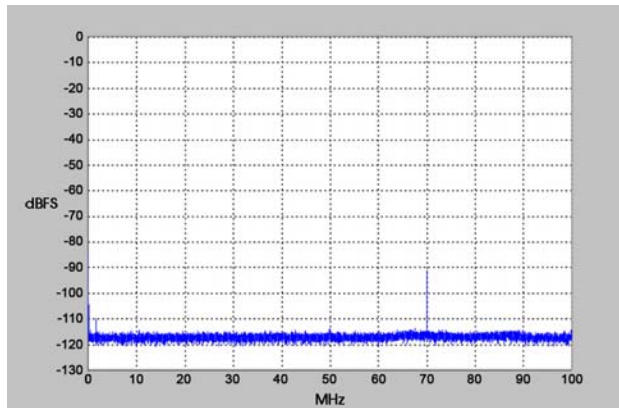
Two-Tone SFDR


 $f_1 = 30 \text{ MHz}, f_2 = 70 \text{ MHz}, f_s = 200 \text{ MHz}$

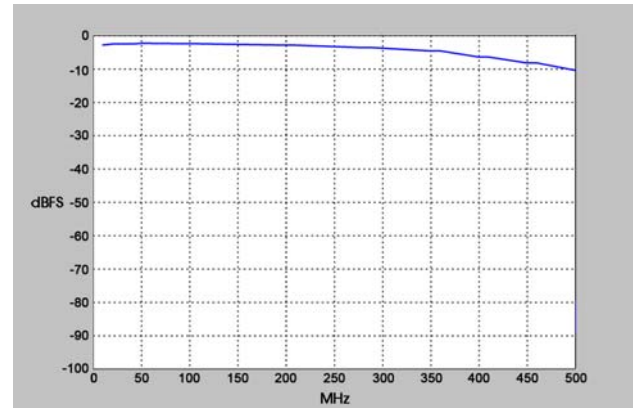
Two-Tone SFDR


 $f_1 = 69 \text{ MHz}, f_2 = 71 \text{ MHz}, f_s = 200 \text{ MHz}$

Adjacent Channel Crosstalk


 $f_{in \text{ Ch2}} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Ch 1 shown}$

Input Frequency Response


 $f_s = 200 \text{ MHz}, \text{Internal Clock}$