General Information

Model 56640 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56640 includes a front panel general-purpose connector for application-specific I/O .

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.
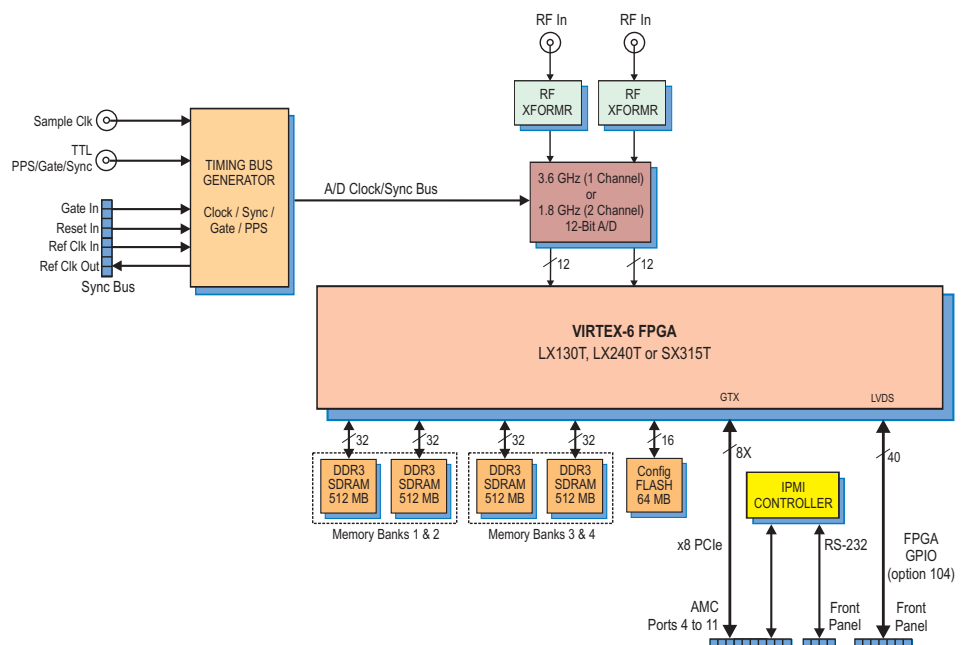
Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O

A/D Acquisition IP Module

The 56640 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

► A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 56640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

The 56640 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple modules to be synchronized, ideal for larger multichanel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 56640's can be synchronized using the Cobalt high speed sync module to drive the sync bus.

Memory Resources

The 56640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module's DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.
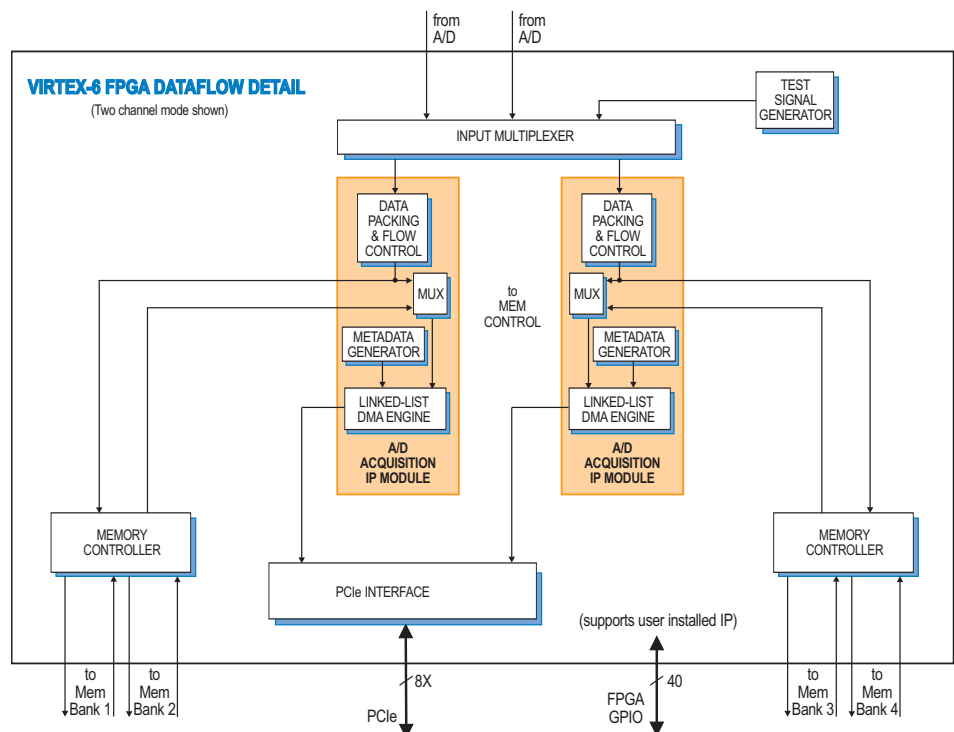
AMC Interface

The Model 56640 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller). ►

VIRTEX-6 FPGA DATAFLOW DETAIL
(Two channel mode shown)

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➤ PCI Express Interface

The Model 56640 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multi-pin connectors, bus includes gate, reset and in and out ref clock

External Trigger Input
Type: Front panel female SSMC connector, TTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2, or XC6VSX315T-2

Custom I/O
Option -104: Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1 or Gen. 2: x4 or x8

AMC Interface
Type: AMC.1
Module Management: IPMI Version 2.0

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model	Description
56640	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - AMC

Options:

-002*	-2 FPGA speed grade
-062	XC6VLX240T
-064	XC6VSX315T
-104	LVDS FPGA I/O through front panel connector
-155*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions