



Model 53720 COTS (left) and rugged version



**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 and 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

**General Information**

Model 53720 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53720 includes three A/Ds, one upconverter, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

**The Onyx Architecture**

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53720 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53720 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

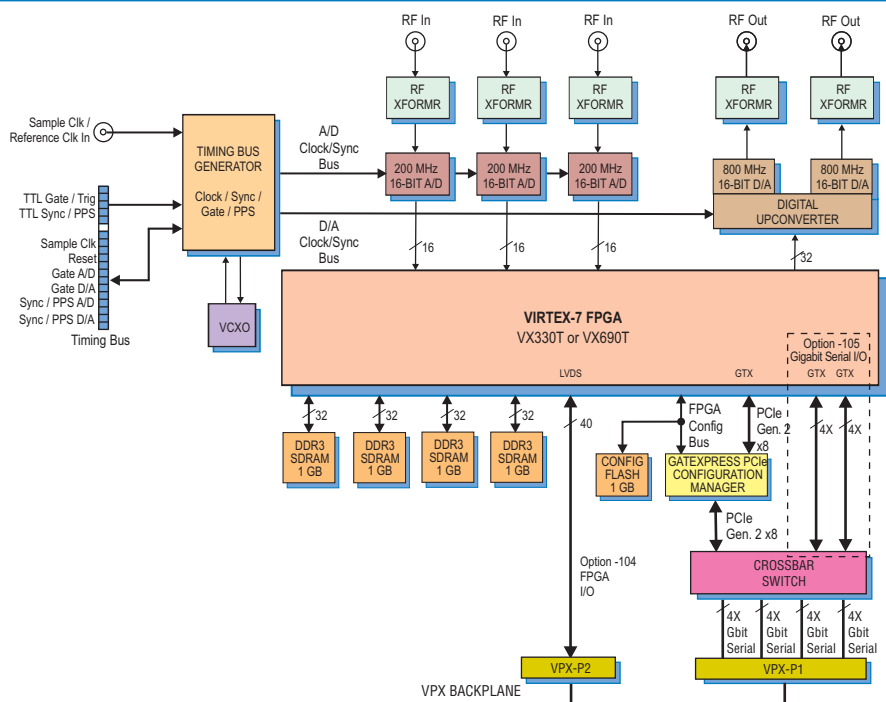
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤



**A/D Acquisition IP Modules**

The 53720 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

**D/A Waveform Playback IP Module**

The Model 53720 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily playback to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

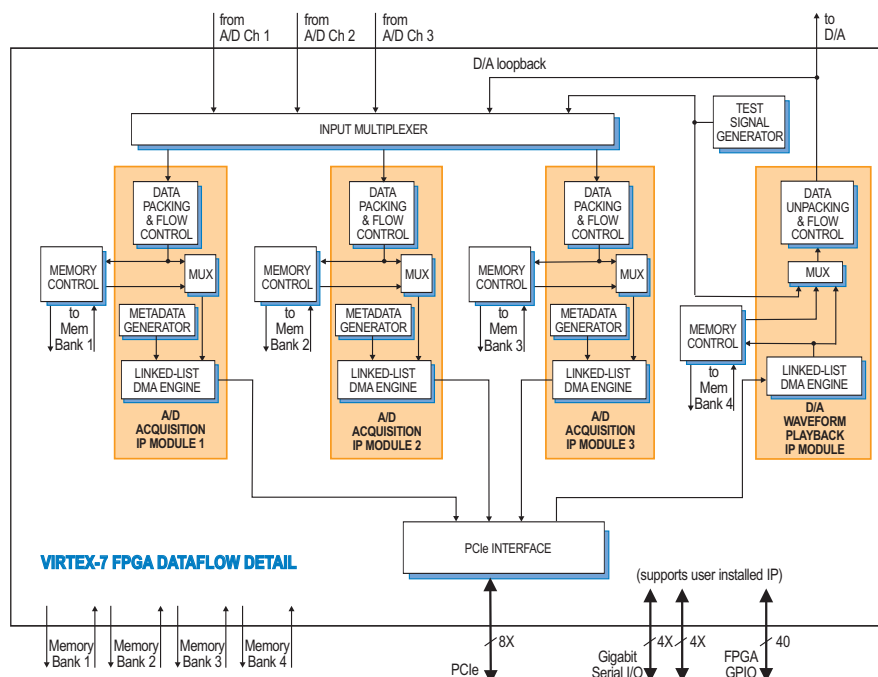
**A/D Converter Stage**

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

**Digital Upconverter and D/A Stage**

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of SSMC connectors. ➤



**Memory Resources**

The 53720 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

**PCI Express Interface**

The Model 53720 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Model 8267**

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.



**Ordering Information**

Model	Description
53720	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-7 FPGA - 3U VPX

**Options:**

-073	XC7VX330T-2 FPGA
-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1

*Contact Pentek for availability of rugged and conduction-cooled versions*

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

► If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable VCXO (Voltage-Controlled Crystal Oscillator).

**Crossbar Switch**

The 53720 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

**Specifications**

**Front Panel Analog Signal Inputs**

**Input Type:** Transformer-coupled, front panel female SSMC connectors  
**Transformer Type:** Coil Craft WBC4-6TLB  
**Full Scale Input:** +8 dBm into 50 ohms  
**3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**

**Type:** Texas Instruments ADS5485  
**Sampling Rate:** 10 MHz to 200 MHz  
**Resolution:** 16 bits

**D/A Converters**

**Type:** Texas Instruments DAC5688  
**Input Data Rate:** 250 MHz max.  
**Output IF:** DC to 400 MHz max.  
**Output Signal:** 2-channel real or 1-channel with frequency translation  
**Output Sampling Rate:** 800 MHz max. with interpolation  
**Resolution:** 16 bits

**Front Panel Analog Signal Outputs**

**Output Type:** Transformer-coupled, front panel female SSMC connectors  
**Transformer:** Coil Craft WBC4-6TLB  
**Full Scale Output:** +4 dBm into 50 ohms  
**3 dB Passband:** 300 kHz to 700 MHz

**Sample Clock Sources:** On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

**Clock Synthesizer**

**Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

**Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

**Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16

**External Clock**

**Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

**Timing Bus:** 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**Field Programmable Gate Array**

**Standard:** Xilinx Virtex-7 XC7VX330T-2  
**Optional:** Xilinx Virtex-7 XC7VX690T-2

**Custom I/O**

**Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

**Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector

**Memory**

**Type:** DDR3 SDRAM  
**Size:** Four banks, 1 GB each  
**Speed:** 800 MHz (1600 MHz DDR)

**PCI-Express Interface**

**PCI Express Bus:** Gen. 1 or Gen. 2: x4 or x8;

**Environmental**

**Operating Temp:** 0° to 50° C

**Storage Temp:** -20° to 90° C

**Relative Humidity:** 0 to 95%, non-cond.

**Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

**VPX Families**

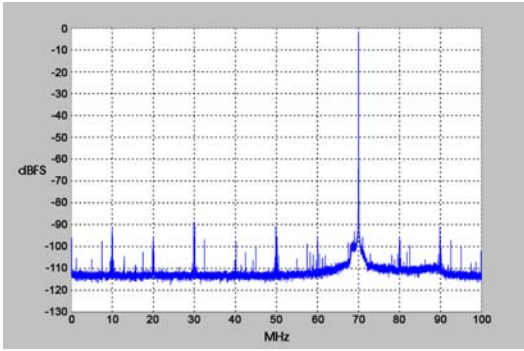
Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison		
	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No



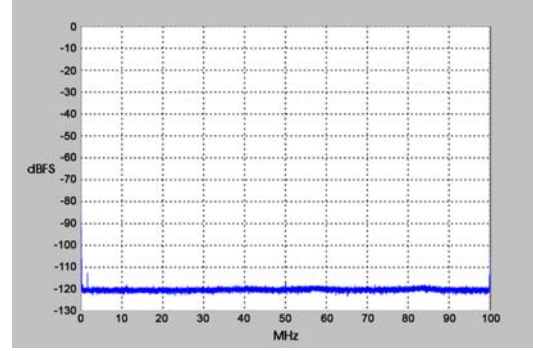
A/D Performance

Spurious Free Dynamic Range



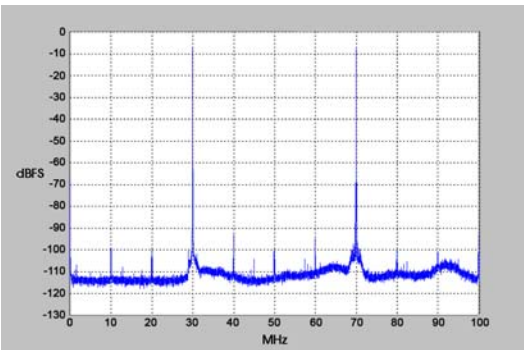
$f_{in} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Internal Clock}$

Spurious Pick-up



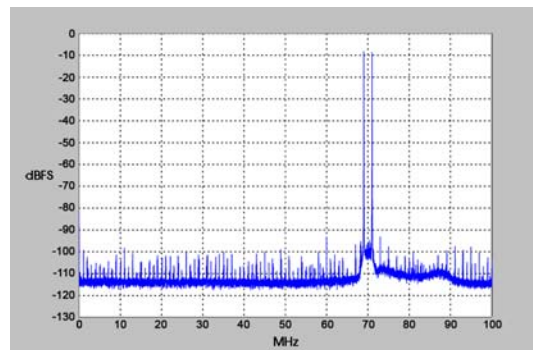
$f_s = 200 \text{ MHz}, \text{Internal Clock}$

Two-Tone SFDR



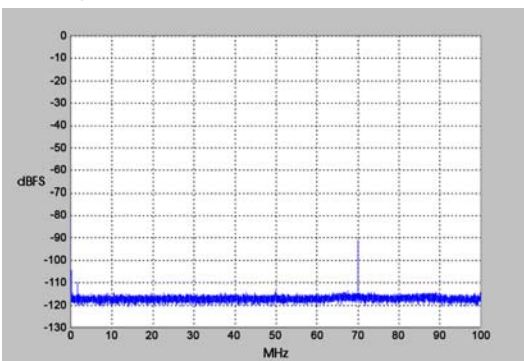
$f_1 = 30 \text{ MHz}, f_2 = 70 \text{ MHz}, f_s = 200 \text{ MHz}$

Two-Tone SFDR



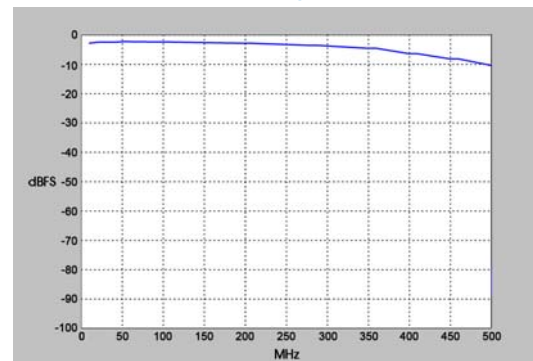
$f_1 = 69 \text{ MHz}, f_2 = 71 \text{ MHz}, f_s = 200 \text{ MHz}$

Adjacent Channel Crosstalk



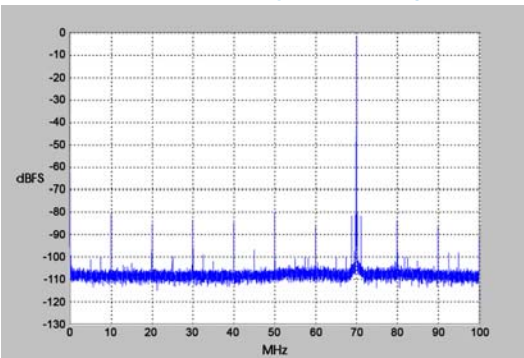
$f_{in \text{ Ch2}} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Ch 1 shown}$

Input Frequency Response



$f_s = 200 \text{ MHz}, \text{Internal Clock}$

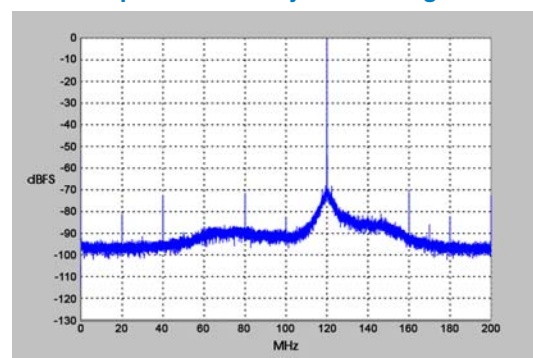
Spurious Free Dynamic Range



$f_{out} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Internal Clock}$

D/A Performance

Spurious Free Dynamic Range



$f_{out} = 140 \text{ MHz}, f_s = 400 \text{ MHz}, \text{External Clock}$